# Homework 4

Max marks: 100

Due on October 21, 2022, 12:00 noon, before class. Please submit in paper, because it is easier to grade. Also submit a backup copy to brightspace. If you are submitting code: submit the code on brightspace; submit compilation and running instructions, test environment, and IO output in paper.

You can choose to implement Quine-McCluskey in your favorite programming language (C, C++, python, javascript etc). Or you can do the following problems by hand. If you use any third-party code, please attribute the third-party code and delineate your code clearly. More than 50% of the code should be your own.

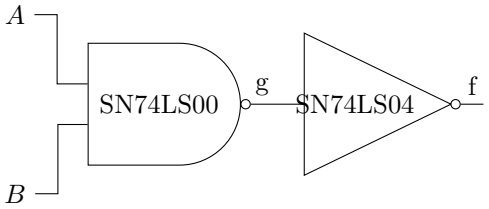
**Problem 1** *Use Quine-McCluskey method to find the minimal SOP for* $f(x, y, z) = \sum m(2, 3, 4, 5)$ *(20 marks)*

**Problem 2** *Use Quine-McCluskey method to find the minimal SOP for* $f(x, y, z, w) = \sum m(0, 1, 4, 5, 12, 13)$ *(20 marks)*

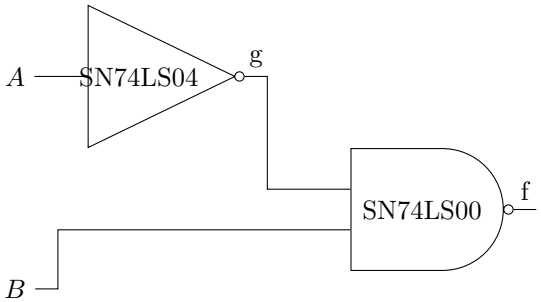
**Problem 3** *Use Quine-McCluskey method to find the minimal SOP for* $f(x, y, z, w) = \sum m(1, 5, 7, 8, 9, 13, 15) + d(4, 14)$ *(20 marks).*

**Problem 4** *Refer to the datasheet of Texas Instrument IC (Integrated circuit) SN74LS00 and SN74LS04. SN74LS00 chip contains four two-input NAND gates. SN74LS04 contains six NOT gates. Find the* $V_{IH}$ *and* $V_{IL}$ *in the "recommended operating conditions" section and* $V_{OH}$ *and* $V_{OL}$ *in the "electrical characteristic" section for both SN74LS00 and SN74LS04. In multiple values are given chose the "TYP" value, because we assume to operate the IC under "NOM" conditions. This is not to test you, but to relate this your knowledge to real world. If you are having trouble finding this information, please email me and I will send you the correct values. The next part is to test your understanding. Find noise margin high and noise margin low for the wire labeled g following circuits (20 marks).*

Circuit A:




Circuit B:




**Problem 5** *Design a 2-input OR gate using*

1. *nMOS transistors (5 marks).*
2. *CMOS technology (5 marks).*
3. *negative logic and CMOS technology (10 marks).*