

# Post-Midterm2 Practice problems

Vikas Dhiman for ECE275

December 5, 2022

**Problem 1** Derive a minimal state table for an FSM (Finite-state machine) that acts as a three-bit parity generator. For every three bits that are observed on the input  $w$  during three consecutive clock cycles, the FSM generates the parity bit  $p = 1$  if and only if the number of 1s in the three-bit sequence is odd (10 marks) [1, Prob 6.12].

**Problem 2** Design a modulo-6 counter, which counts in the sequence 0, 1, 2, 3, 4, 5, 0, 1, . . . . The counter counts the clock pulses if its enable input,  $w$ , is equal to 1. Use D flip-flops in your circuit (20 marks) [1, Prob 6.23].

**Problem 3** Design a three-bit counterlike circuit controlled by the input  $w$ . If  $w = 1$ , then the counter adds 2 to its contents, wrapping around if the count reaches 8 or 9. Thus if the present state is 8 or 9, then the next state becomes 0 or 1, respectively. If  $w = 0$ , then the counter subtracts 1 from its contents, acting as a normal down-counter. Use J-K flip-flops in your circuit (20 marks) [1, Prob 6.26].

## State Reduction

**Problem 4** Reduce the following state table to a minimum number of states:

Present State	Next State		Present Output (Z)
	X = 0	1	
a	e	e	1
b	c	e	1
c	i	h	0
d	h	a	1
e	i	f	0
f	e	g	0
g	h	b	1
h	c	d	0
i	f	b	1

(10 marks).

**Problem 5** Digital engineer B. I. Nary has just completed the design of a sequential circuit which has the following state table:

Present State	Next State		Output	
	X = 0	1	0	1
$S_0$	$S_5$	$S_1$	0	0
$S_1$	$S_5$	$S_6$	0	0
$S_2$	$S_2$	$S_6$	0	0
$S_3$	$S_0$	$S_1$	1	0
$S_4$	$S_4$	$S_3$	0	0
$S_5$	$S_0$	$S_1$	0	0
$S_6$	$S_5$	$S_1$	1	0

His assistant, F. L. Ipfflop, who has just completed this course, claims that his design can be used to replace Mr. Nary's circuit. Mr. Ipfflop's design has the following state table:

	Next State		Output	
	X = 0	1	0	1
<b>a</b>	<b>a</b>	<b>b</b>	<b>0</b>	<b>0</b>
<b>b</b>	<b>a</b>	<b>c</b>	<b>0</b>	<b>0</b>
<b>c</b>	<b>a</b>	<b>b</b>	<b>1</b>	<b>0</b>

1. Is Mr. Ipfflop correct? (Prove your answer.)(10 marks)
2. If Mr. Nary's circuit is always started in state  $S_0$ , is Mr. Ipfflop correct? (Prove your answer by showing equivalent states, etc.) (10 marks)

### State Assignment

- Problem 6**
1. Reduce the following state table to a minimum number of states using implication charts (10 marks).
  2. Use the guideline method to determine a suitable state assignment for the reduced table (10 marks).
  3. Realize the table using D flip-flops (10 marks).
  4. Realize the table using J-K flip-flops (10 marks).

	$X = 0$	1	Z
A	A	B	1
B	C	E	0
C	F	G	1
D	C	A	0
E	I	G	1
F	H	I	1
G	C	F	0
H	F	B	1
I	C	E	0

### Design using Multiplexer

**Problem 7** Figure 1 shows the notation for a BCD to 7-segment display and Table 1 shows the corresponding truth table. The inputs corresponding to the missing rows in the truth table should be considered as don't care.

1. implement segment "a" using an 8:1 mux and no other logic gate, (10 marks)
2. implement segment "a" using a 4:1 mux and one other gate, (10 marks)
3. implement segment "f" with 4:1 mux and no other logic gate. Assume inputs are available in both uncomplemented and complemented form. (Hint: There are  ${}^4C_2 = 6$  possible pairs of control inputs:  $(w_3, w_2)$ ,  $(w_2, w_1)$ ,  $(w_1, w_0)$ ,  $(w_0, w_3)$ ,  $(w_0, w_2)$ ,  $(w_1, w_3)$ . There are 6 don't care conditions. With two control inputs of the multiplexer and one input, you can represent an expression with up to 4-SOP-terms of size three-literals or less. You might arrive at the answer sooner, if you try to write the minimal SOP expression first and find the two inputs that occur most often in all the terms. Those two inputs are most likely to be the chosen pair of control inputs.) (10 marks)

**Problem 8** Consider the function  $f = \bar{w}_2\bar{w}_3 + w_1w_2$ . Derive a circuit for  $f$  that uses only one 2-to-1 multiplexer and no other gates (assuming inputs are available in both uncomplemented and complemented form). [1, Prob 4.4](10 marks)

### Design using Decoder

**Problem 9** Show how the function  $f(w_1, w_2, w_3) = \sum m(0, 2, 3, 4, 5, 7)$  can be implemented using a 3-to-8 binary decoder and an OR gate. [1, Prob 4.1] (10 marks)

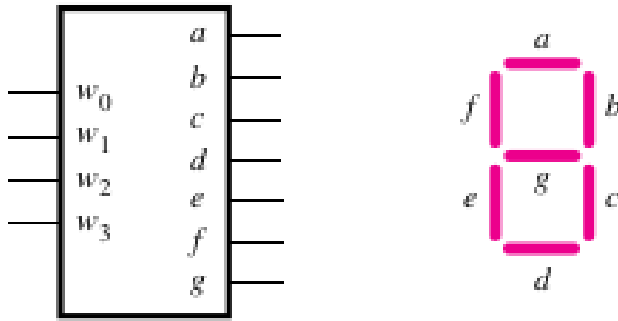


Figure 1: Seven segment display and BCD-to-7-segment display converter. When  $a = 1$  the corresponding segment of the display lights up. To display the number 8, you will turn on all the seven segments, while to display 1, you will turn on  $b = 1, c = 1$  and turn off  $= 0$  the rest. The full truth-table for the seven-segment display is shown in Table 1.

Row	$w_3$	$w_2$	$w_1$	$w_0$	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Table 1: Truth table for BCD to seven-segment display as shown in Figure 1. The missing combinations of inputs should be considered as dont care.

## References

- [1] S. Brown and Z. Vranesic. *Fundamentals of Digital Logic with Verilog Design: Third Edition*. McGraw-Hill Higher Education, 2013.