Analog details behind the digital abstraction

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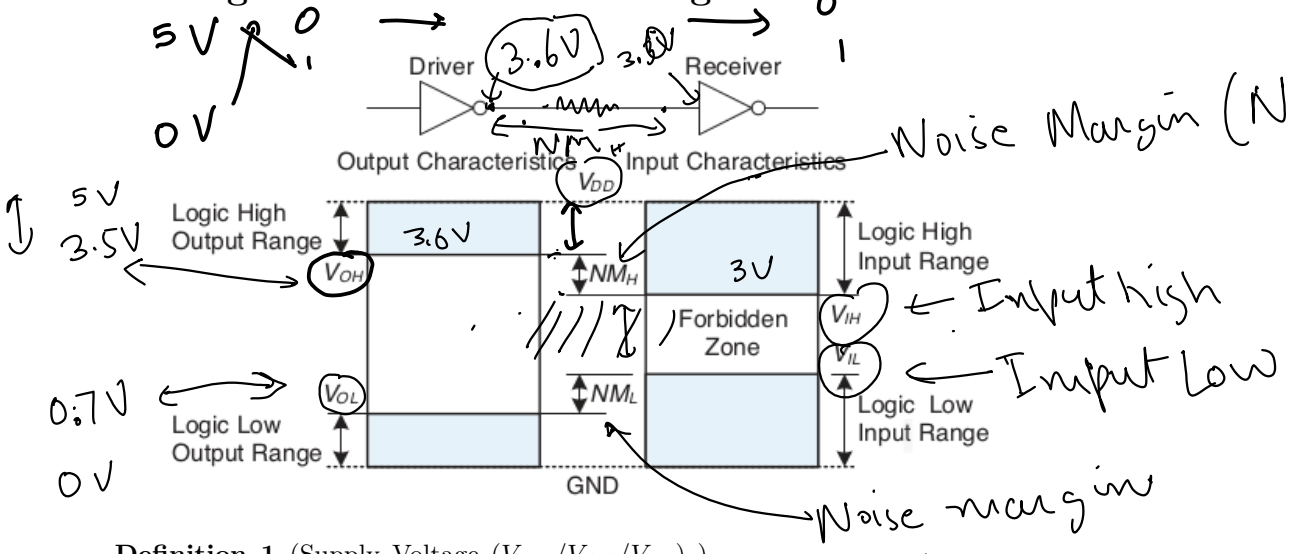
Some of the material is out of the textbook. Additional resources include Appendix B of Brown and Vranesic book, "Fundamentals of digital logic."

1 Objectives

1. Describe how tri-state and open-collector outputs are different from totem-pole outputs
2. Compute noise margin of one device driving the same time
3. Understand timing diagrams, gate delays and critical path
4. Design Hazard-free two level circuits

2 Logic levels and Noise Margins



Definition 1 (Supply Voltage ($V_{DD}/V_{CC}/V_{SS}$)).

Definition 2 (Ground Voltage (V_{GND})).

Definition 3 (Input high (V_{IH}) and Input Low (V_{IL}) of a gate).

0 - 5V

minimum

$V_{IH} = 2.5V$

$V_{IL} = 2.5V$

$V_{OH} = 5V$

$V_{OL} = 0V$

Definition 4 (Output high (V_{OH}) and Output low (V_{OL}) of gate).

V_{OH} is the voltage that the gate will output for a "HIGH" output

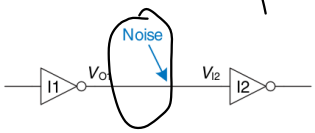
Definition 5 (Positive logic and Negative logic).

Definition 6 (Noise margins (NM_L and NM_H) of a channel).

$NM_H = |V_{OH} - V_{IH}| > 0$

$NM_L = |V_{IL} - V_{OL}| > 0$

fan-out capacity



Example 1.
If $V_{DD} = 5V$, $V_{IL} = 1.35V$, $V_{IH} = 3.15V$, $V_{OL} = 0.33V$ and $V_{OH} = 3.84V$ for both the "inverters", then what are the low and high noise margins? Can the circuit tolerate 1V of noise at the channel?

$NM_H = V_{OH} - V_{IH} = 3.84 - 3.15 = 0.69V$

$NM_L = V_{IL} - V_{OL} = 1.35 - 0.33 = 1.02V$

3 Semiconductors and Doping

Not in syllabus but good to know

Elements recognized as metalloids V • T • E

	13	14	15	16	17
2	B Boron	C Carbon	N Nitrogen	O Oxygen	F Fluorine
3	Al Aluminium	Si Silicon	P Phosphorus	S Sulfur	Cl Chlorine
4	Ga Gallium	Ge Germanium	As Arsenic	Se Selenium	Br Bromine
5	In Indium	Sn Tin	Sb Antimony	Te Tellurium	I Iodine
6	Tl Thallium	Pb Lead	Bi Bismuth	Po Polonium	At Astatine

Commonly recognized (86–99%): B, Si, Ge, As, Sb, Te
Irregularly recognized (40–49%): Po, At
Less commonly recognized (24%): Se
Rarely recognized (8–10%): C, Al
(All other elements cited in less than 6% of sources)
Arbitrary metal-nonmetal dividing line: between
Be and B, Al and Si, Ge and As, Sb and Te, Po and At

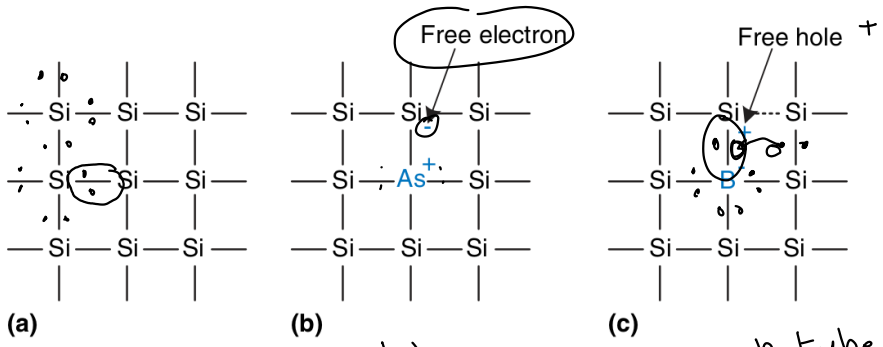
Metal

Non metal

Si 2,8,4

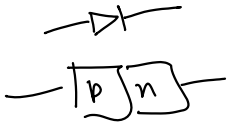
6.

Adding impurities → n-type As
Doping → p-type B



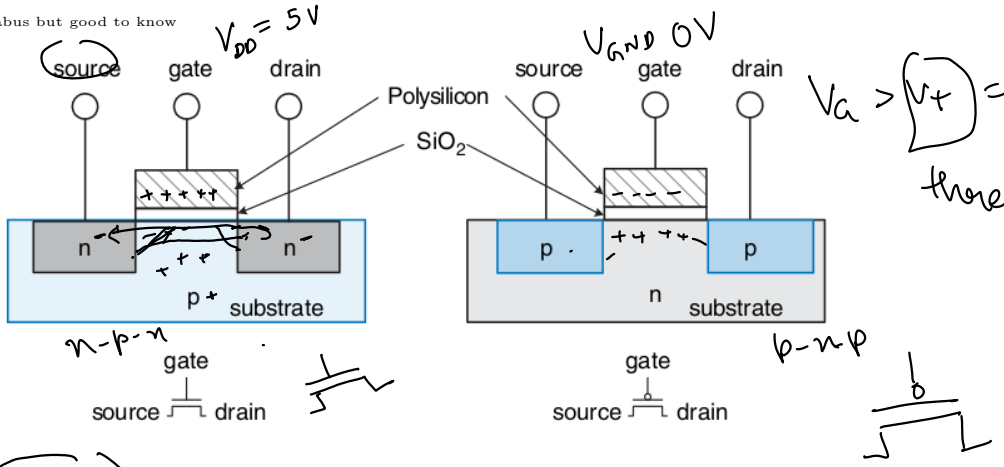
n-type semiconductor

p-type semiconductor



4 MOSFET: Metal Oxide Field Effect Transistors

Not in syllabus but good to know



$V_{DD} = 5V$

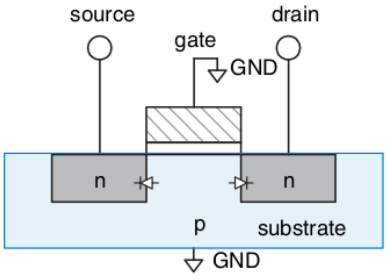
V_{GND} 0V

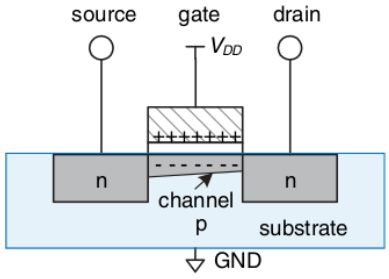
$V_a > |V_t| = 0.7V$

threshold voltage

n-p-n

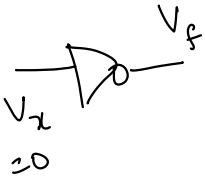
p-n-p

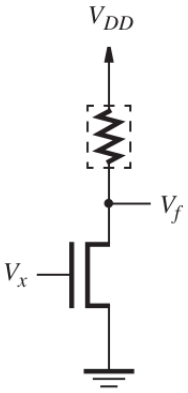




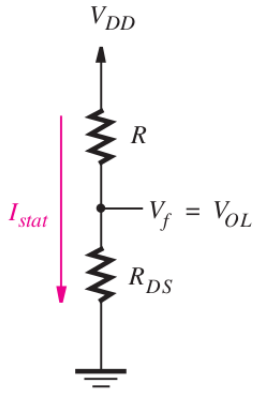
nMOS operation

5 DC Transfer characteristic

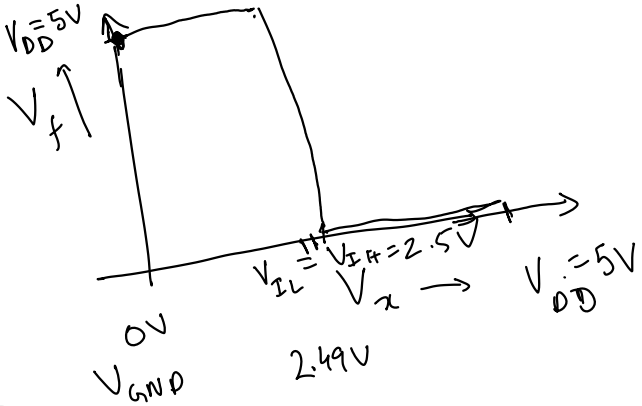




(a) NMOS NOT gate



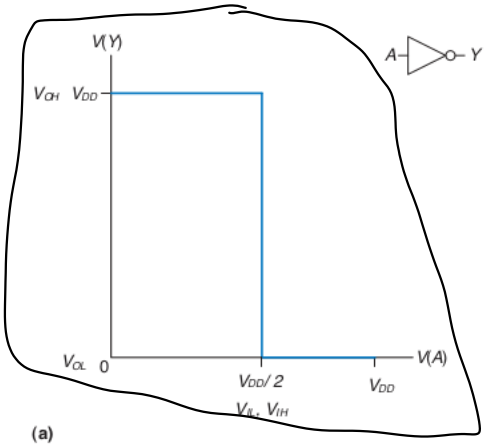
(b) $V_x = 5$ V

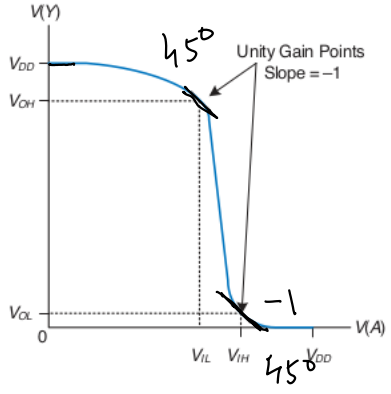


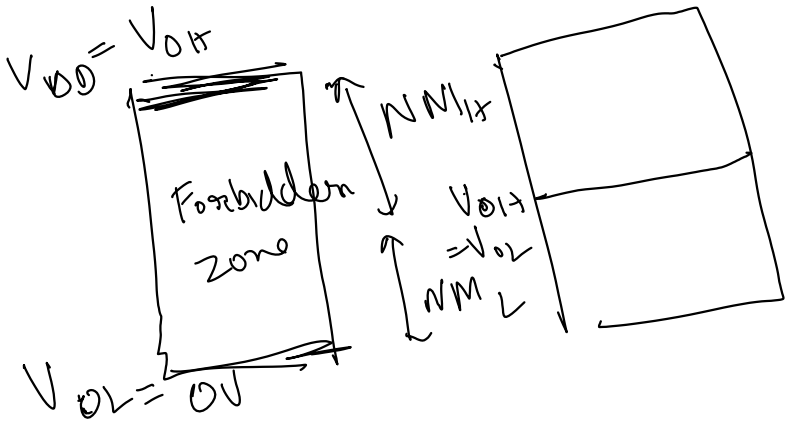
L → H

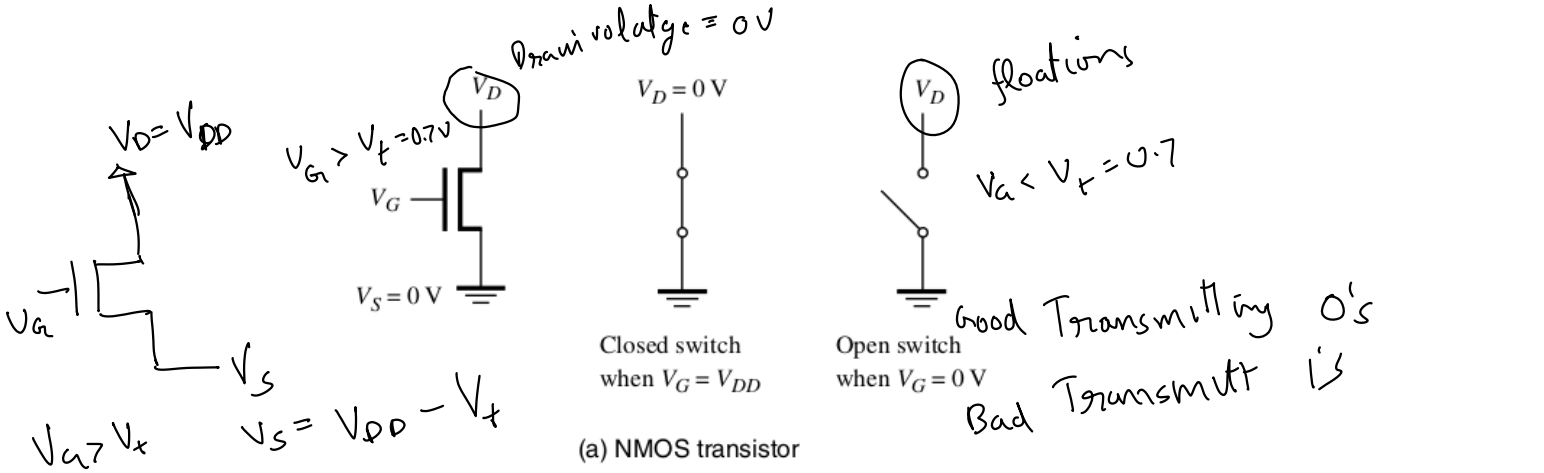
H → L

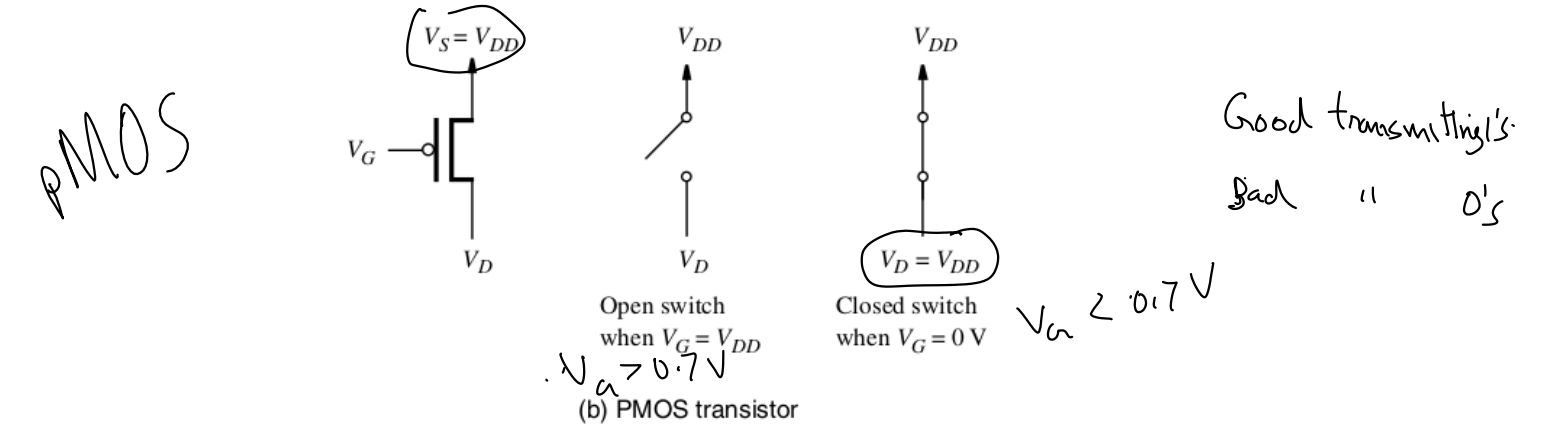
$V_{IL} = V_{IH} = 2.5$



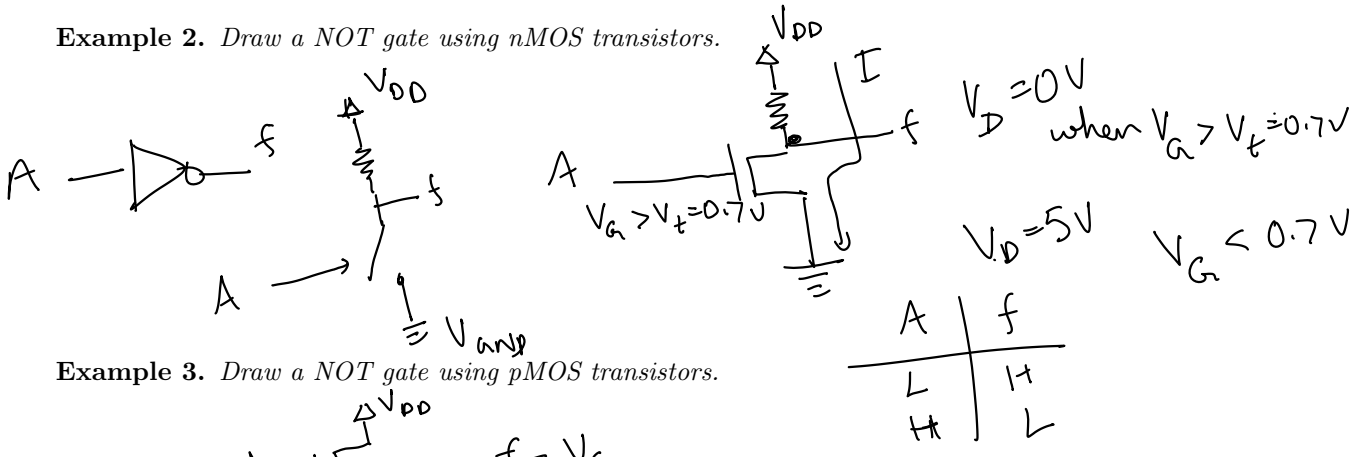




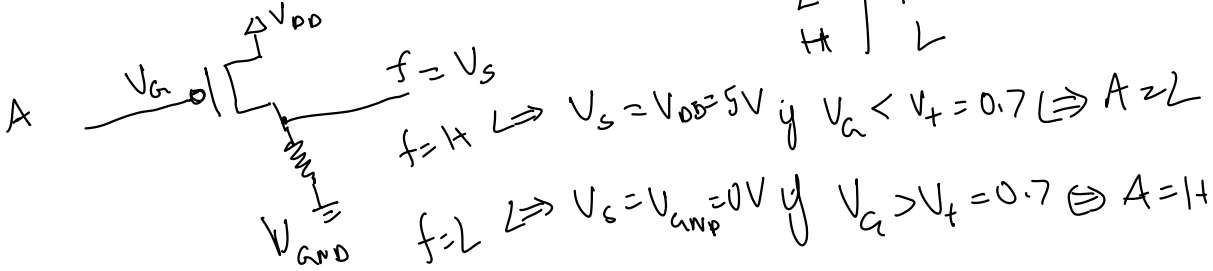




Example 2. *Draw a NOT gate using nMOS transistors.*



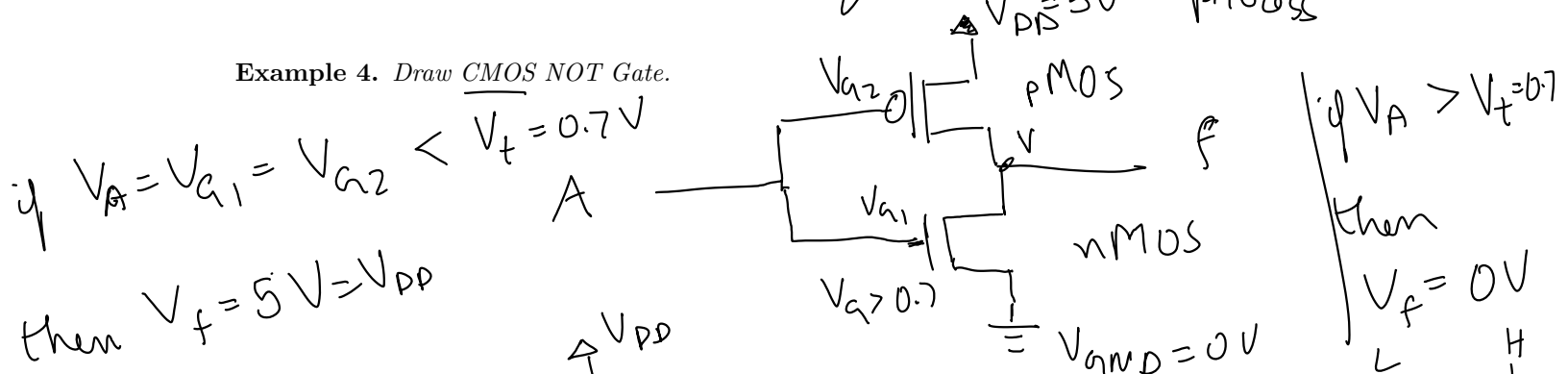
Example 3. *Draw a NOT gate using pMOS transistors.*



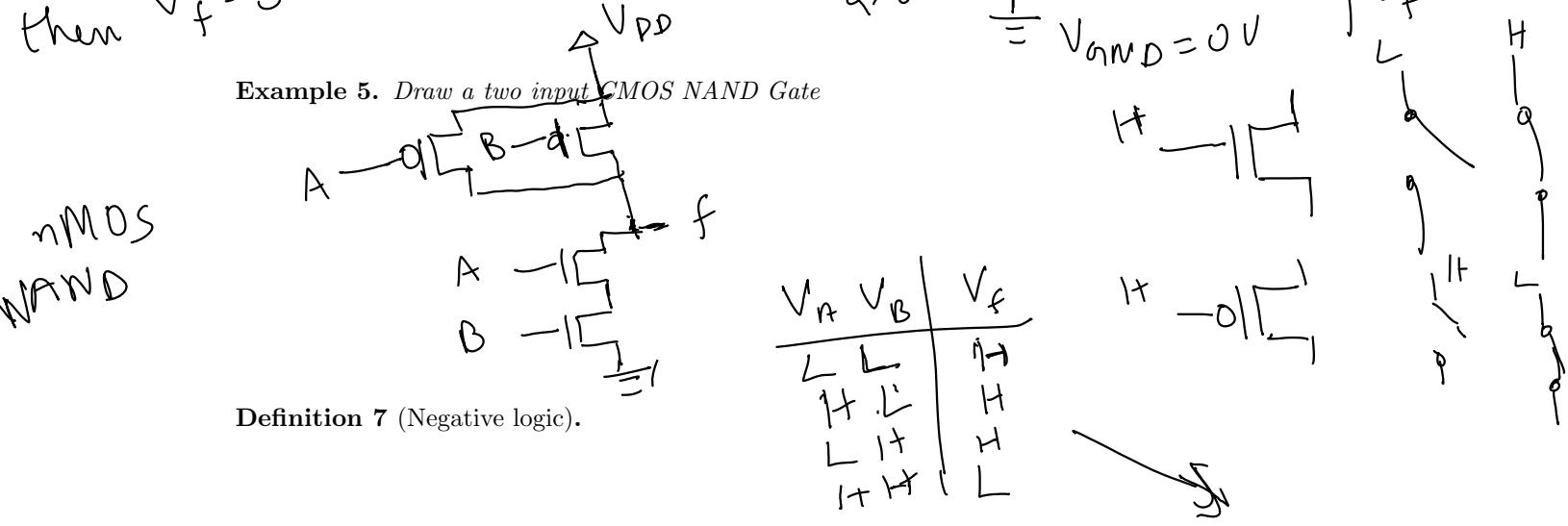
Remark 1. *nMOS transistors pass 0's well (output between 0 and $V_{DD} - V_t$). pMOS transistors pass 1's well (output between V_t and V_{DD}).*

CMOS - complimentary MOS technology

Example 4. *Draw CMOS NOT Gate.*



Example 5. *Draw a two input CMOS NAND Gate*



V_A	V_B	V_f
L	L	H
H	L	H
L	H	H
H	H	L

Definition 7 (Negative logic)**.**

Example 6. *Analyze the above circuit under negative logic.*

Positive logic H = 1 , L = 0

Negative logic H = 0 , L = 1

V_A	V_B	V_f
L	L	H
L	H	H
H	L	H
H	H	L

Example 7. *Draw a three input NAND using CMOS.*

Pos Logic

NAND gate

A	B	f
0	0	1
0	1	1
1	0	1
1	1	0

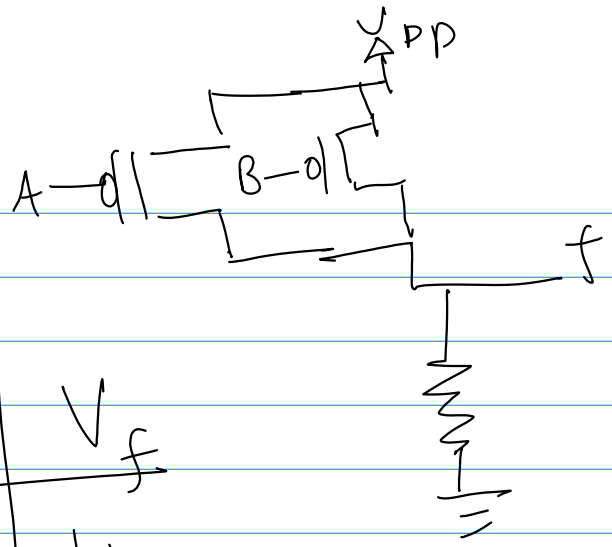
A	B	f
1	1	0
1	0	0
0	1	0
0	0	1

-ve logic

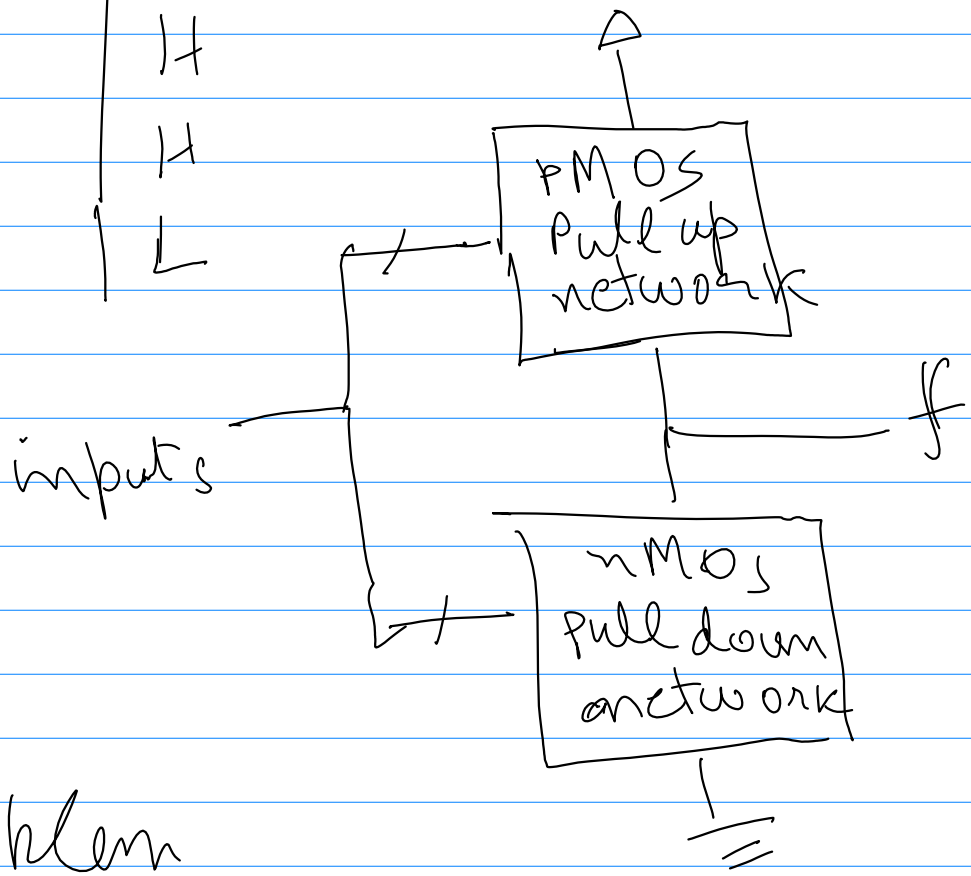
NOR gate

Example 8. *Draw a three input NOR using CMOS.*

pMOS



V_A	V_B	V_f
L	L	H
L	H	H
H	L	H
H	H	L



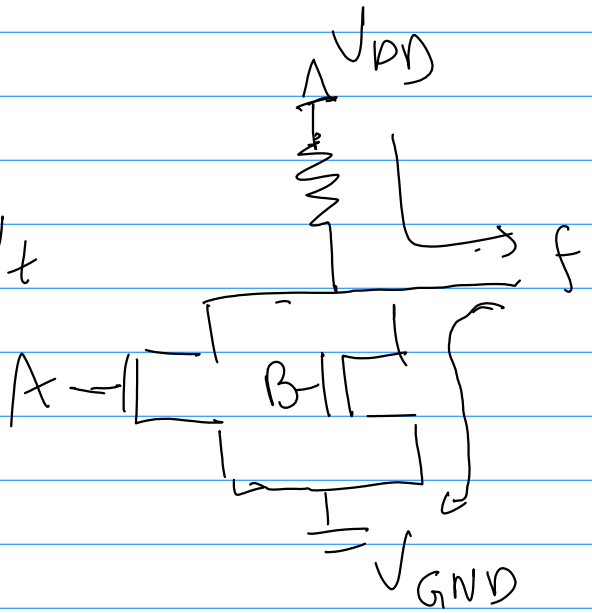
Practice problem

two input NOR gate using CMOS

nMOS

V_A	V_B	V_f
L	L	H
L	H	L
H	L	L
H	H	L

$V_{DD} - V_t$

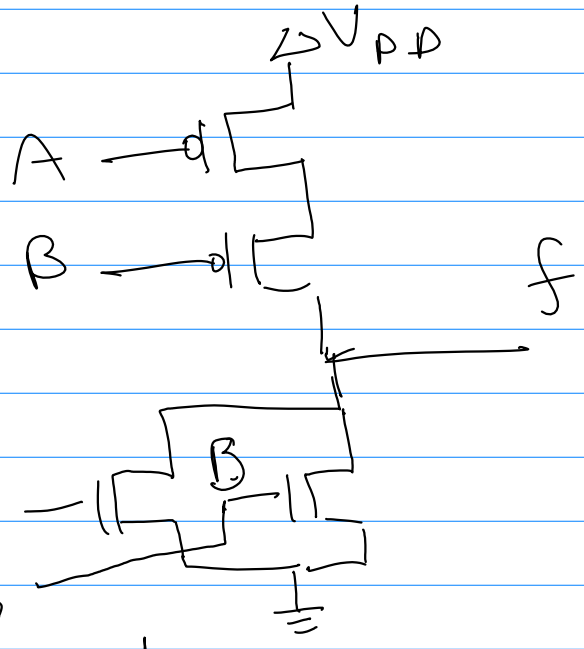


NOR gate

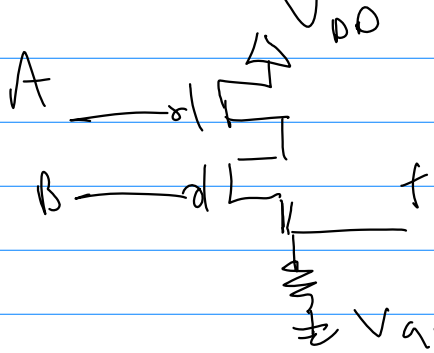
nMOS is bad at transmitting 1's.

bMOS

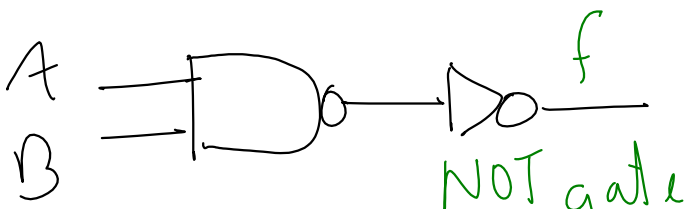
CMOS NOR gate

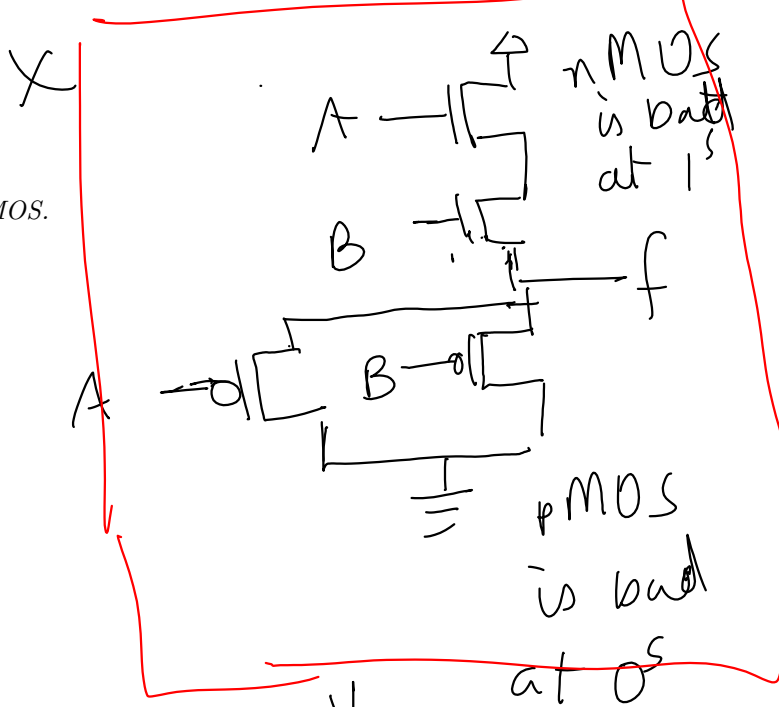


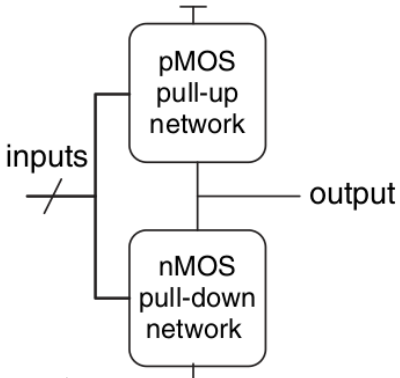
V_A	V_B	V_f
L	L	H
L	H	L
H	L	L
H	H	L



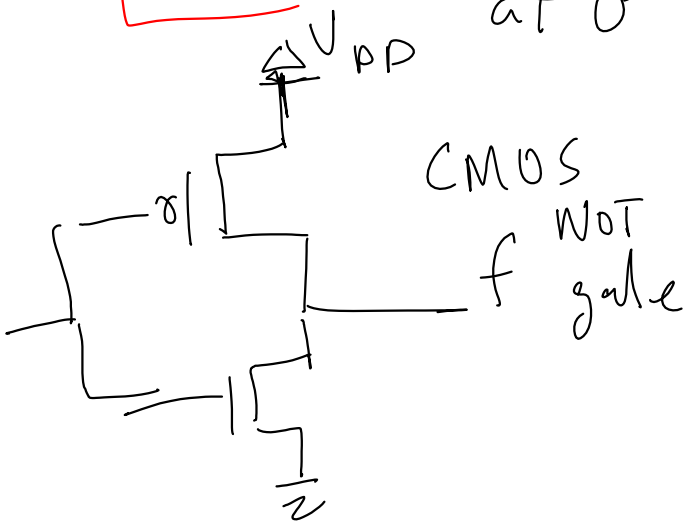
Example 9. *Draw a two input AND gate using CMOS.*





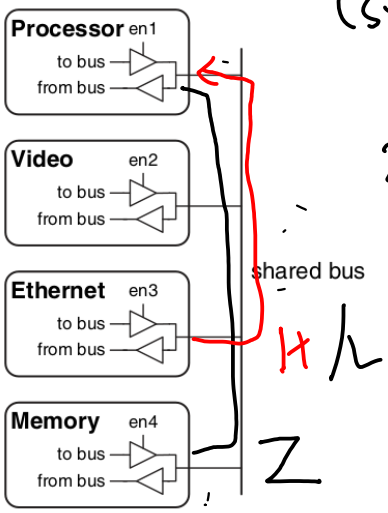


High impedence



5.1 Gates with floating output

(section 1.7.7, 2.6.2)

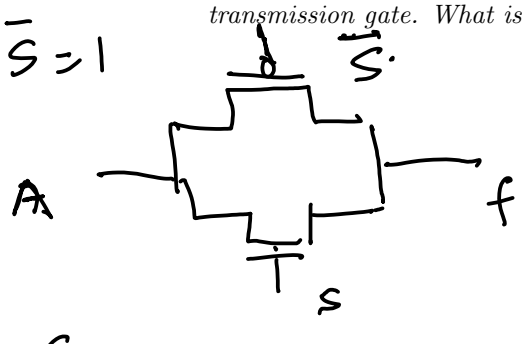


H and L

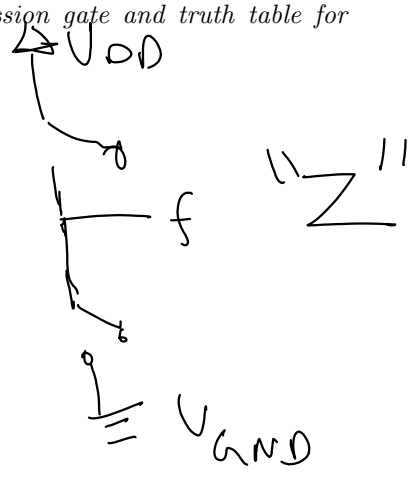
and high impedence state or floating output

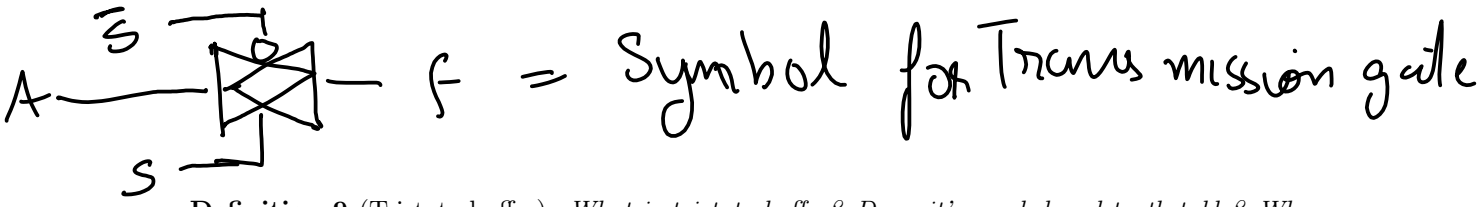
circuit

Definition 8 (Transmission gate). *Draw a schematic of transmission gate and truth table for transmission gate. What is its commonly used symbol?*

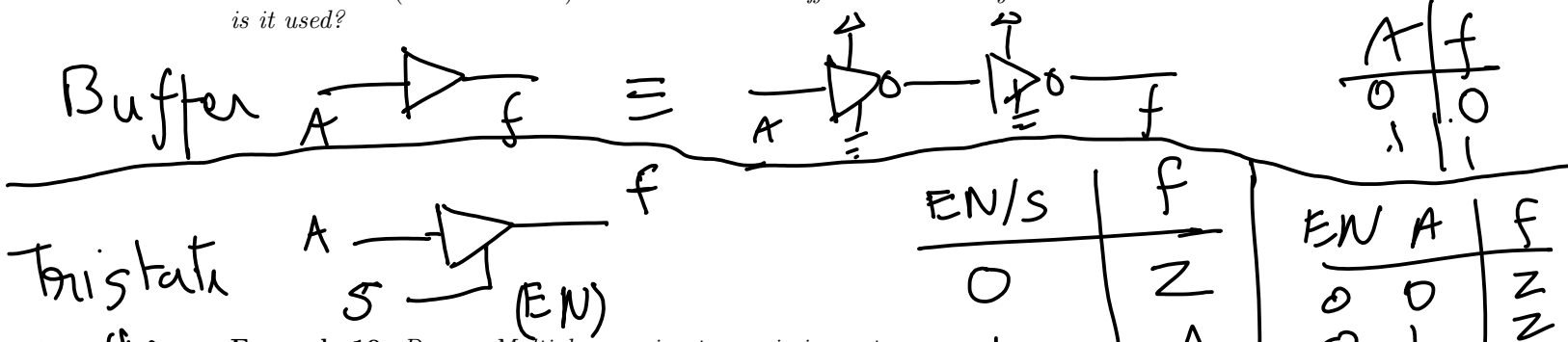


S	A	f
0	0	Z
0	1	Z
1	0	0
1	1	1

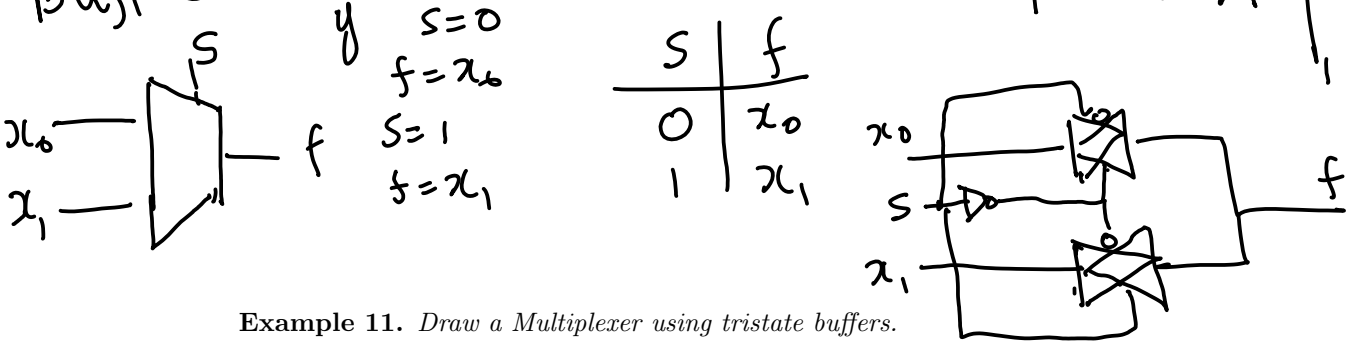




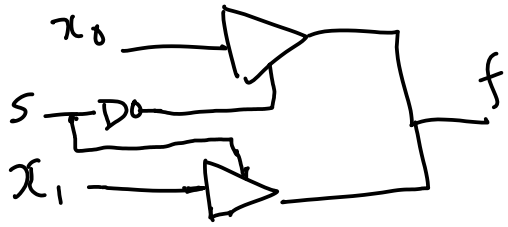
Definition 9 (Tristate buffer)**.** *What is tristate buffer? Draw it's symbol and truth table? Where is it used?*



Example 10. *Draw a Multiplexer using transmission gates.*



Example 11. *Draw a Multiplexer using tristate buffers.*

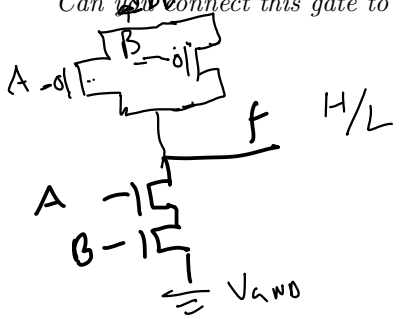


Totempole (Push-pull)

vs Tristate

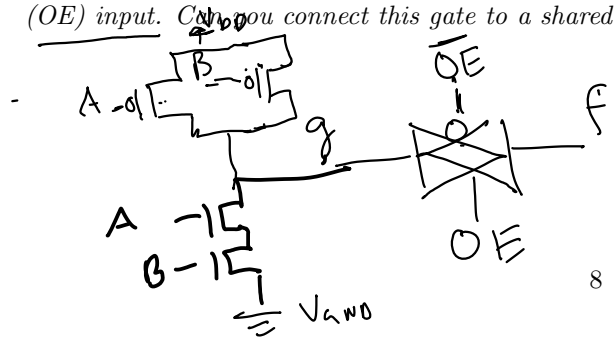
vs open collector

Definition 10 (Totem-pole)**.** *Draw a Push-pull (or Totem-pole) output NAND gate using CMOS. Can you connect this gate to a shared bus?*



Output

Definition 11 (Tristate)**.** *Draw a Tristate output NAND gate using CMOS with an output enable (OE) input. Can you connect this gate to a shared bus?*



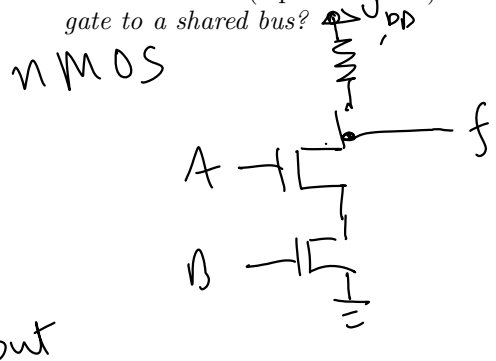
OE | f
0 | Z
1 | A·B

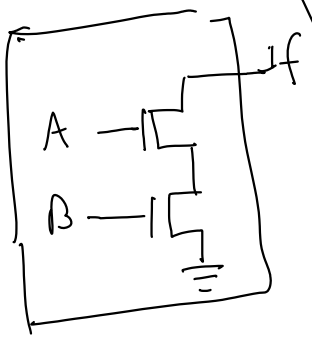
f H/L Z

Open-collector

pseudo-nMOS (section 1.7.8)

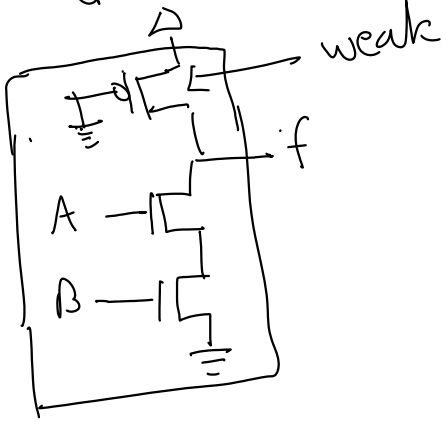
Definition 12 (Open-collector). *Draw a open-collector output NAND gate. Can you connect this gate to a shared bus?*





A	B	f
0	0	Z
0	1	Z
1	0	Z
1	1	0

Push-pull output



6 Verilog truth tables

0, 1, Z, X

invalid

Table 11-11—Bitwise binary AND operator

&	0	1	x	z
0	0	0	0	0
1	0	1	x	x
x	0	x	x	x
z	0	x	x	x

Table 11-12—Bitwise binary OR operator

|	0	1	x	z
0	0	1	x	x
1	1	1	1	1
x	x	1	x	x
z	x	1	x	x

7 Timing diagrams and propagation delays

Example 12 (Timing diagram). *Draw a timing diagram for an ideal NAND gate.*

f = A & B

0 & x

0 & z

&	0	1	x	z
0	0	0	0	0
1	0	1	x	x
x	0	x	x	x
z	0	x	x	x

f = A | B

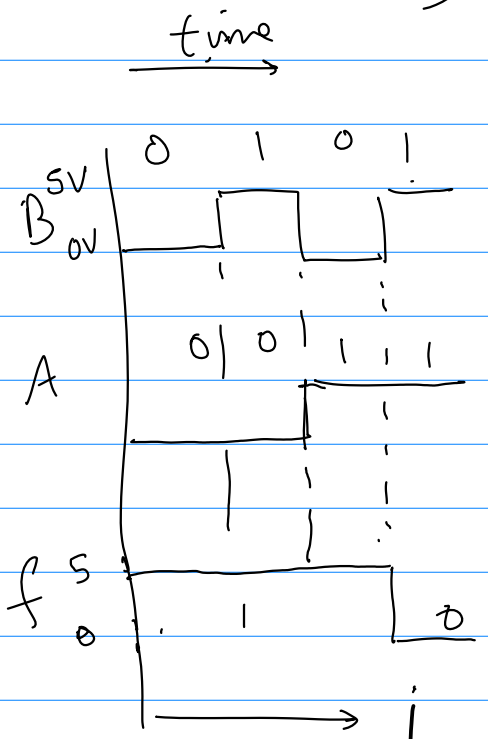
f = 1 | x

|	0	1	x	z
0	0	1	x	x
1	1	1	1	1
x	x	1	x	x
z	x	1	x	x

Timing diagrams (section 2.9)

Ideal timing diagram NAND

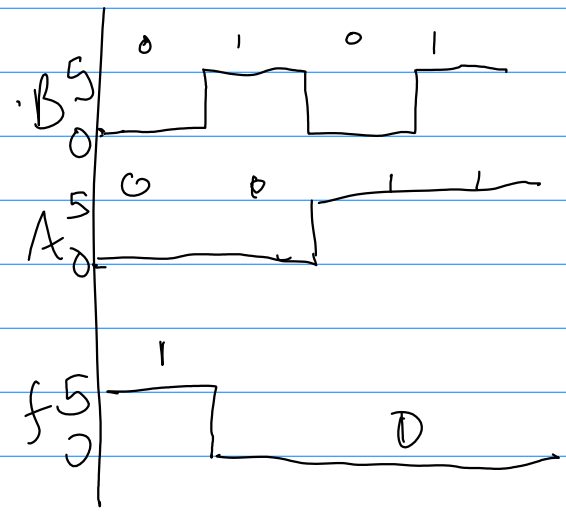
A	B	f
0	0	1
0	1	1
1	0	1
1	1	0



Timing diagram

Ideal NOR gate

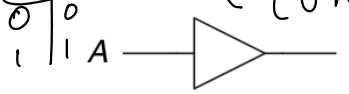
A	B	f
0	0	1
0	1	0
1	0	0
1	1	0

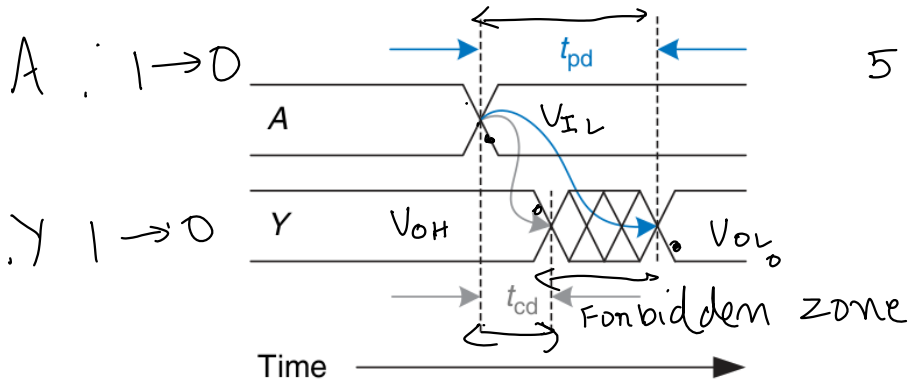


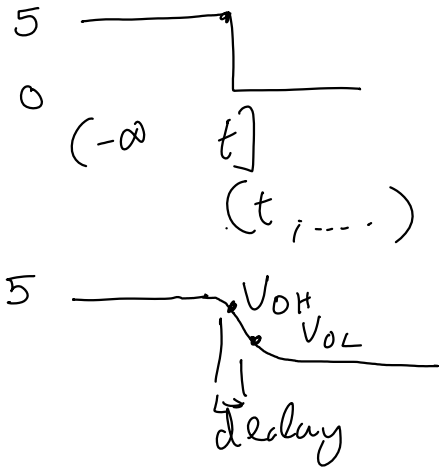
7.1 Delays

propagation

contamination







Definition 13 (Propagation delay (t_{pd})).

Time delay between change in input to a stabalized desired output

Definition 14 (Contamination delay (t_{cd})).

Time delay between change in input to any change in output

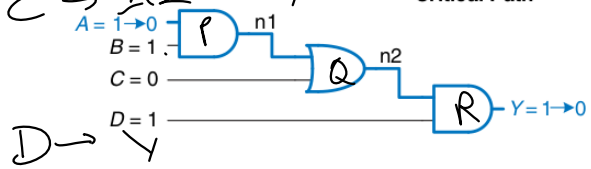
Any sequence of elements through which signal flows from inputs to outputs

7.2 Paths

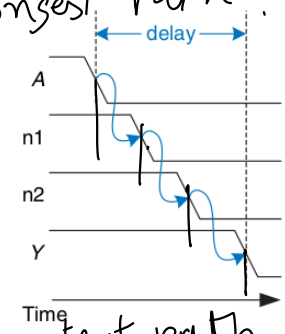
A → n1 → n2 → Y

C → n2 → Y

D → Y

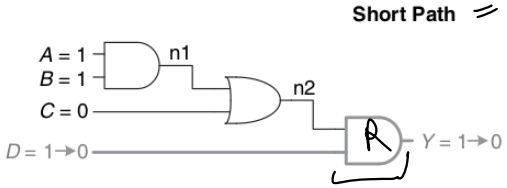


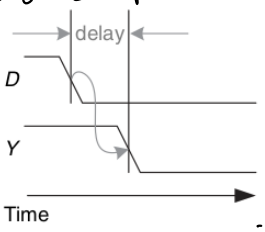
Critical Path = longest path



propagation delay along the critical path of a circuit is the propagation delay of the circuit

Short Path = shortest path





t_{cd} of a circuit is the summation of all t_{cd} s along the shortest path

Example 13. *Find the propagation delay of the circuit above given that propagation delay of each gate is* 100*ps* ~~and~~ *contamination delay of* 60*ps*.

$t_{pd} = t_{pd}(P) + t_{pd}(Q) + t_{pd}(R)$

$= 300\ ps$

$t_{cd} = ? = 60\ ps = t_{cd}(R)$

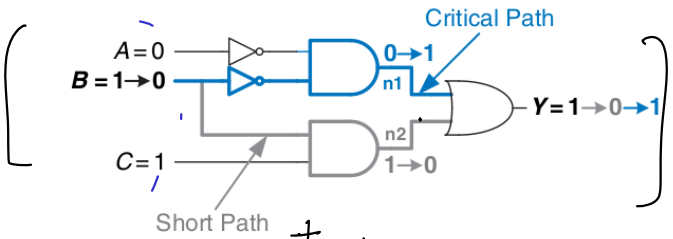
8 Glitches or Hazards

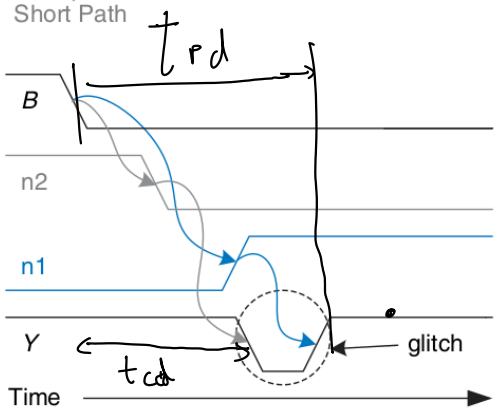
Synchronous circuits → CLOCK → of any circuit element is measured at CLOCK intervals

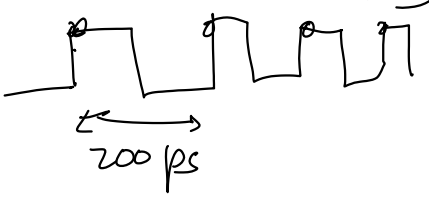
↓ or

Asynchronous circuits

Output







CLK period > t_{pd}

DONT worry about glitches

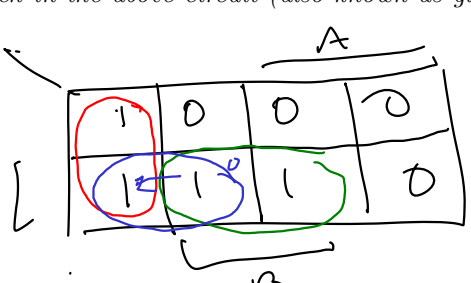
Definition 15 (Glitch or Hazard).

Temporary change in output of a circuit due to difference in signal time delay in different paths of the circuit

Example 14. *Design a circuit that fixes the glitch in the above circuit (also known as glitch-free or hazard-free circuit).*

$Y = \bar{A}\bar{B} + BC$

Glitch = Groups touch but do not overlap



Glitch free circuit = $Y = \bar{A}\bar{B} + BC + \bar{A}C$