Sequential logic design

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1 Objectives

1. Analyse and design both Mealy and Moore sequential circuits with multiple inputs and multiple outputs
2. Convert between Mealy and Moore designs

2 Mealy vs Moore Finite State Machines

Definition 1 (Finite State Machines (FSM))**.** *[1, Sec 3.4]*

FSM is another name for sequential circuits.
FSM is defined in opposition to Infinite State Machines (Turing Machines).

Definition 2 (Mealy FSM)**.** *[1, Sec 3.4.3]*

Mealy FSM have outputs that depend up on both inputs and the state of the circuit or the FSM.

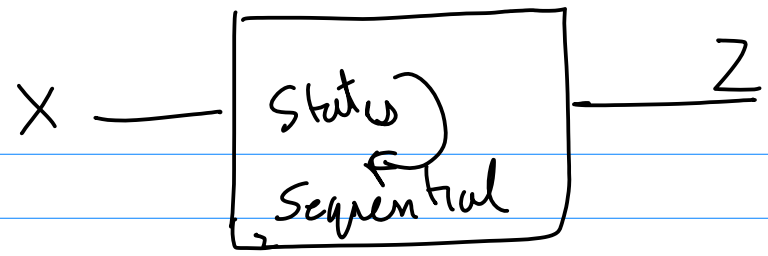
Definition 3 (Moore FSM)**.** *[1, Sec 3.4.3]*

Moore FSM have outputs that depend only upon the states of the FSM.

seq detector

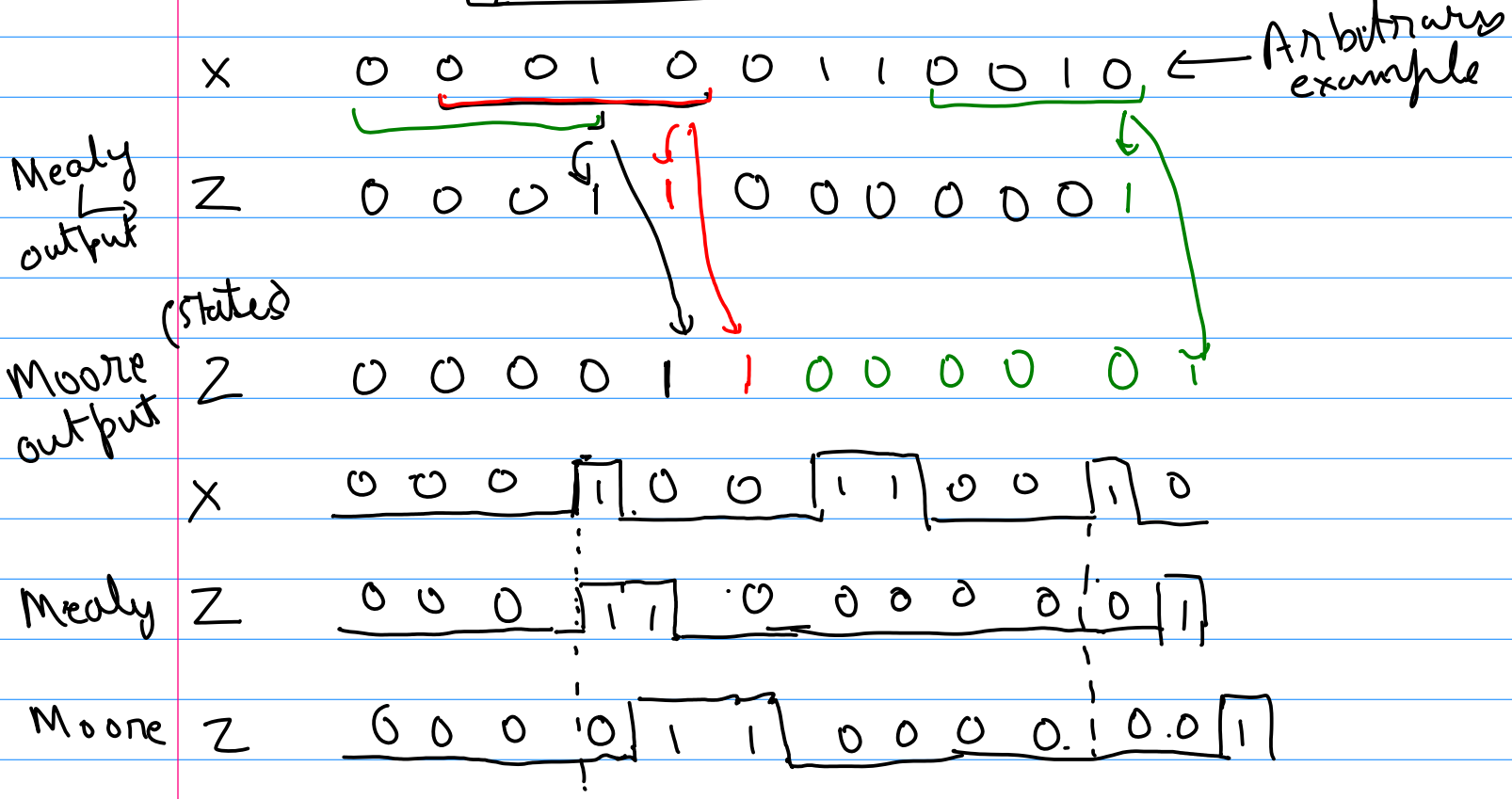
Example 1. *A sequential circuit has one input (X) and one output (Z). The circuit examines groups of four consecutive inputs and produces an output Z=1 if the input sequence 0010 or 0001 occurs. The sequences can overlap. Draw both Mealy and Moore timing diagrams. Find the Mealy and Moore state graph.*

0010
0001



0 0 1 0
0 0 0 1
Z = 1

otherwise Z = 0



Mealy FSM

Output depends on both state + input

Moore FSM

Output depends on state only

Practice Problem 1. *A sequential circuit has one input (X) and one output (Z). The circuit examines groups of four consecutive inputs and produces an output Z=1 if the input sequence 0101 or 1001 occurs. The circuit resets after every four inputs. Draw both Mealy and Moore timing diagrams. Find the Mealy and Moore state graph.*

Inputs

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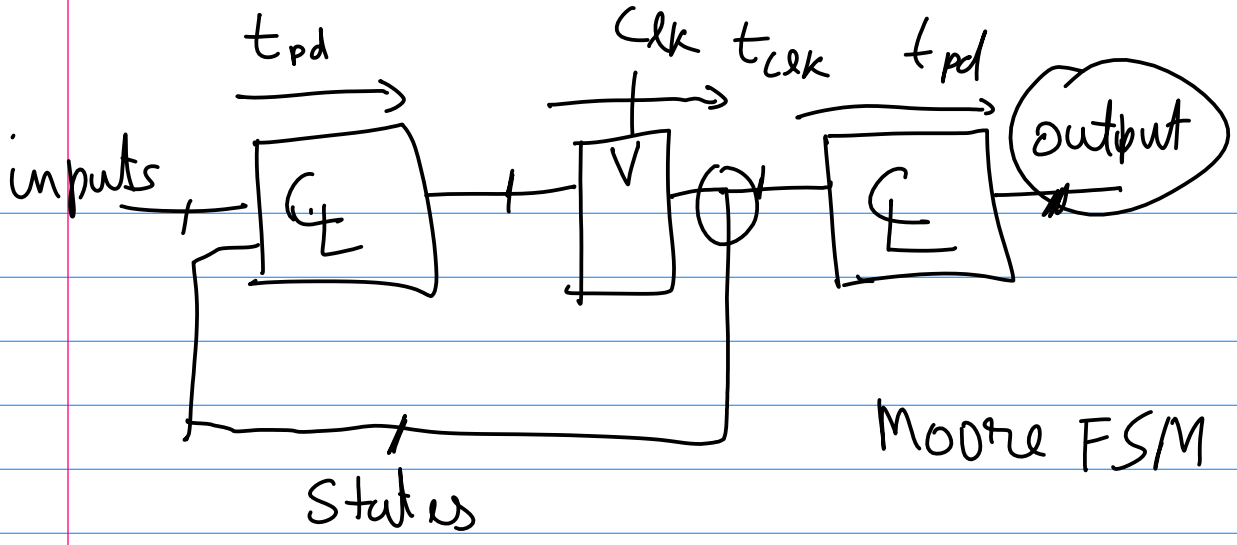
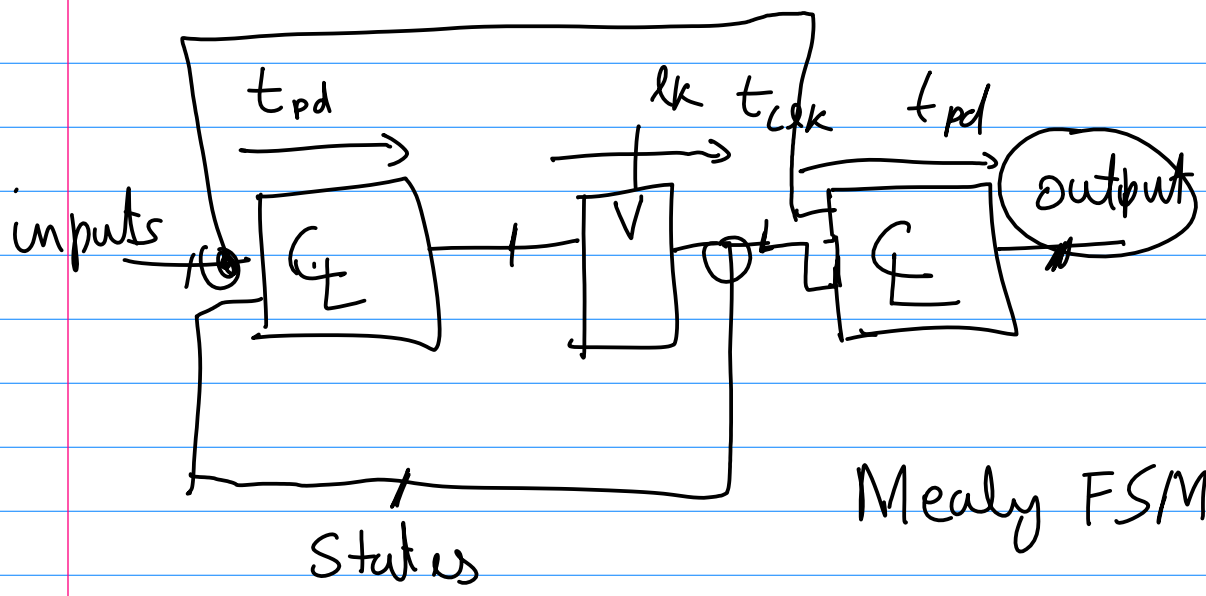
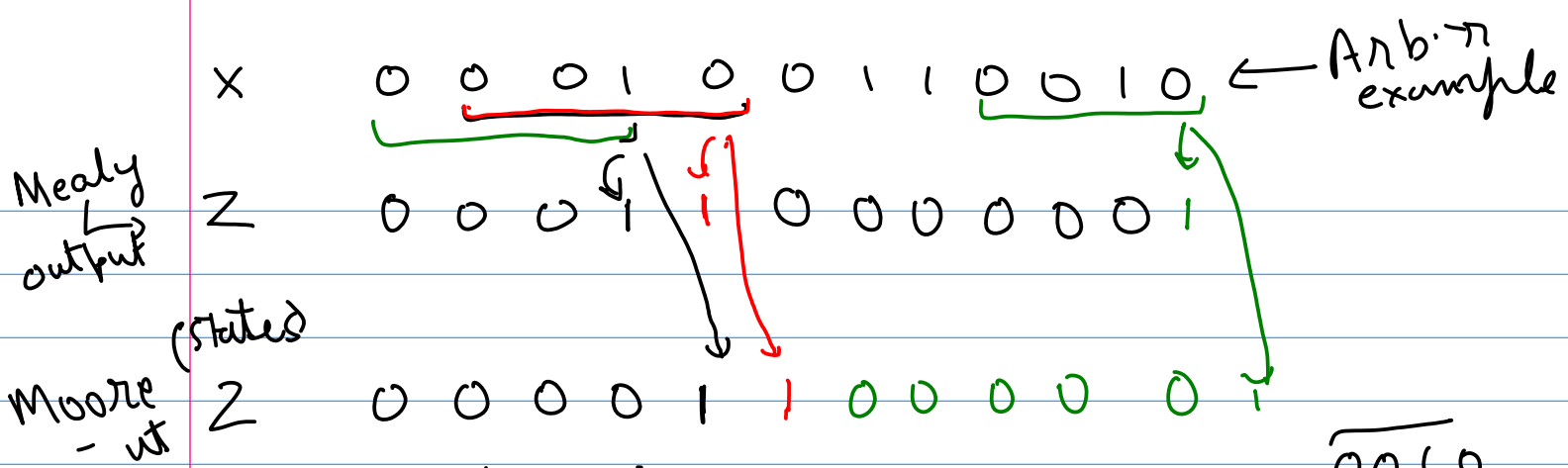
References

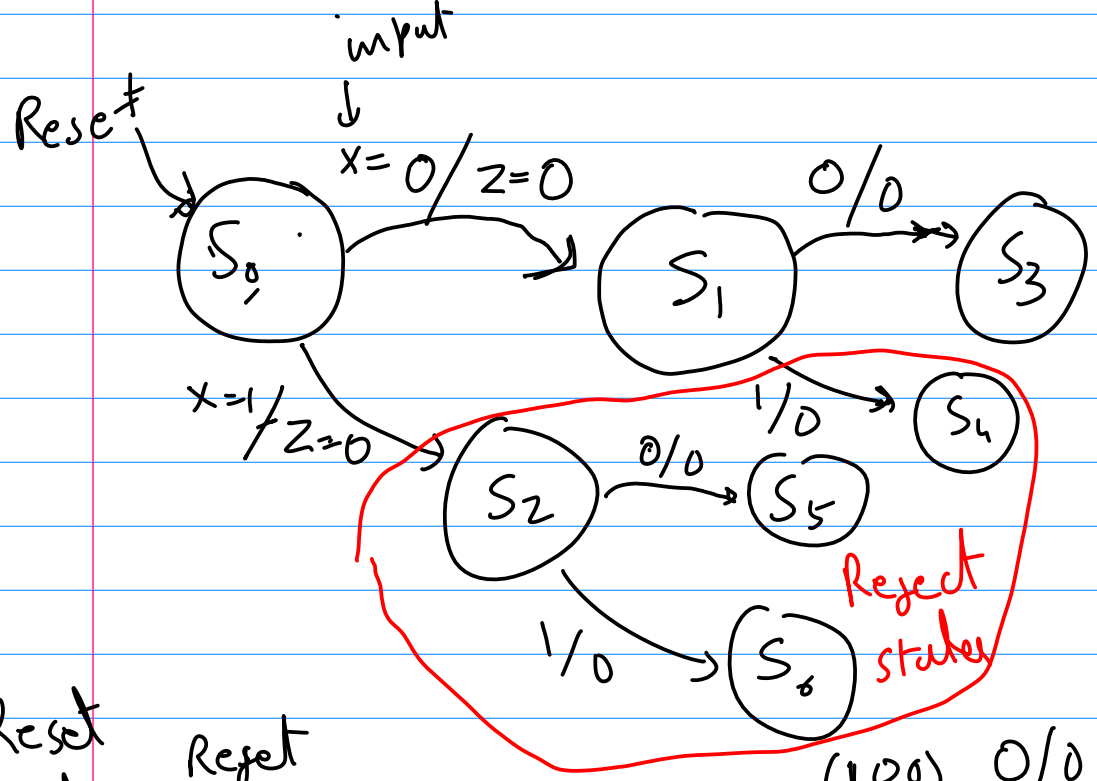
[1] Sarah L Harris and David Harris. *Digital design and computer architecture*. Morgan Kaufmann, 2022.

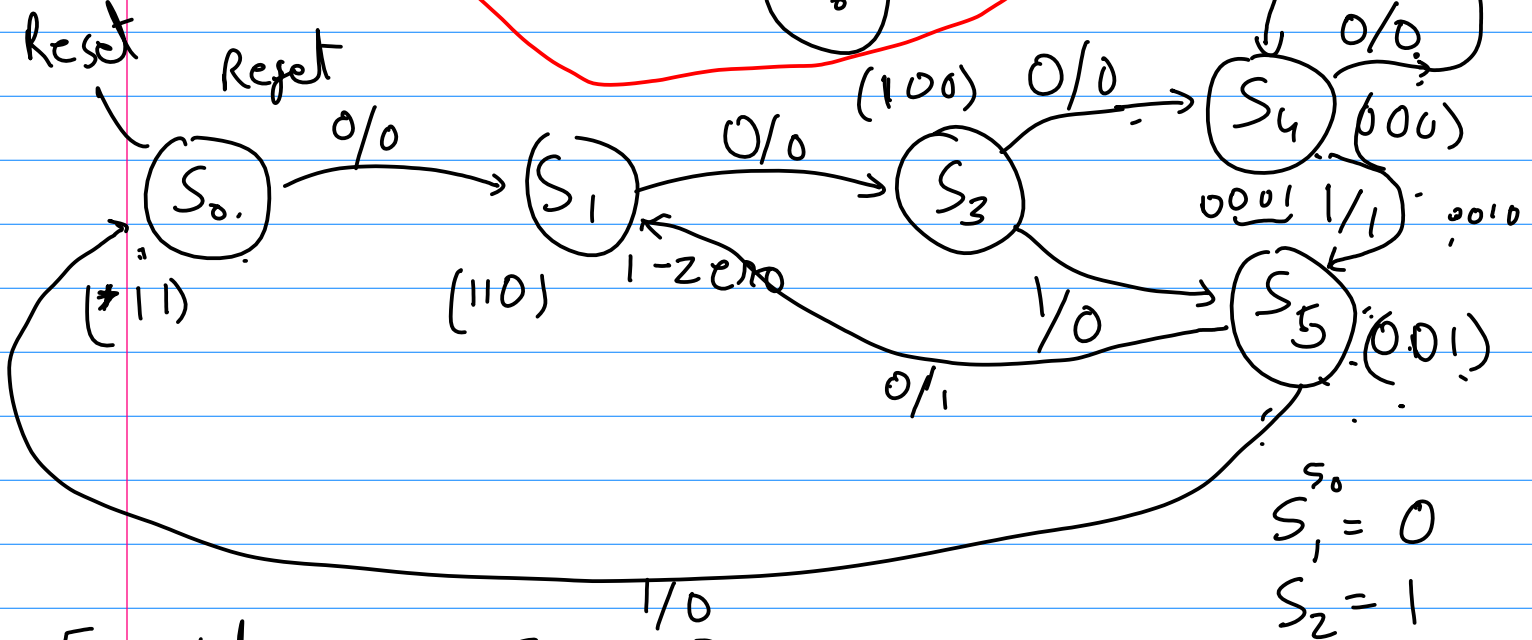

t_{pd}
Clk t_{clk}
t_{pd}
inputs
CL
V
CL
output
Moore FSM
States


t_{pd}
Clk t_{clk}
t_{pd}
inputs
CL
V
CL
output
Mealy FSM
States



Mealy state diagram





5 -states # FF = 3

0010
0001

S_0 =

$S_1 = 0$

$S_2 = 1$

$S_3 = 00$

$S_4 = 01$

$S_5 = 10$

$S_6 = 11$

S_0

$S_1 = 0$

$S_2 = 1$

$S_3 = 00$

$S_4 = 000$

$S_5 = 001$

(1) Word problem

↓

(2) FSM (Mealy / Moore)

↓

(3) State transition table

↓

(4) State assignment $S_0 = 000$

(5) Using $\begin{bmatrix} D\text{-ff} \\ T\text{-ff} \\ JK\text{-ff} \end{bmatrix}$, design a circuit

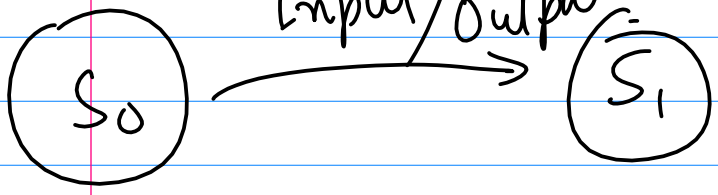
(5.a) Use an excitation table

(5.b) Truth table that maps from inputs + state to the ff inputs

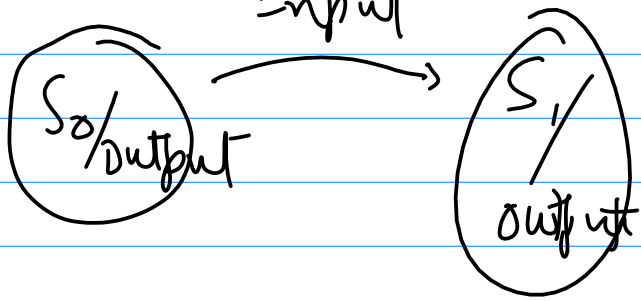
(5.c) TT input + states → output
state → output

① Draw a Moore FSM for detecting [0010 or 0001] with overlap

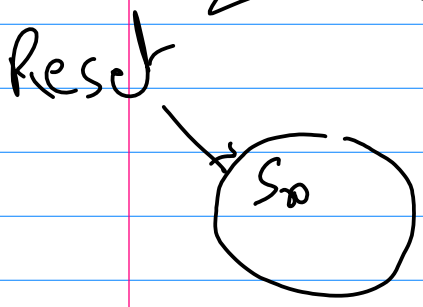
Mealy

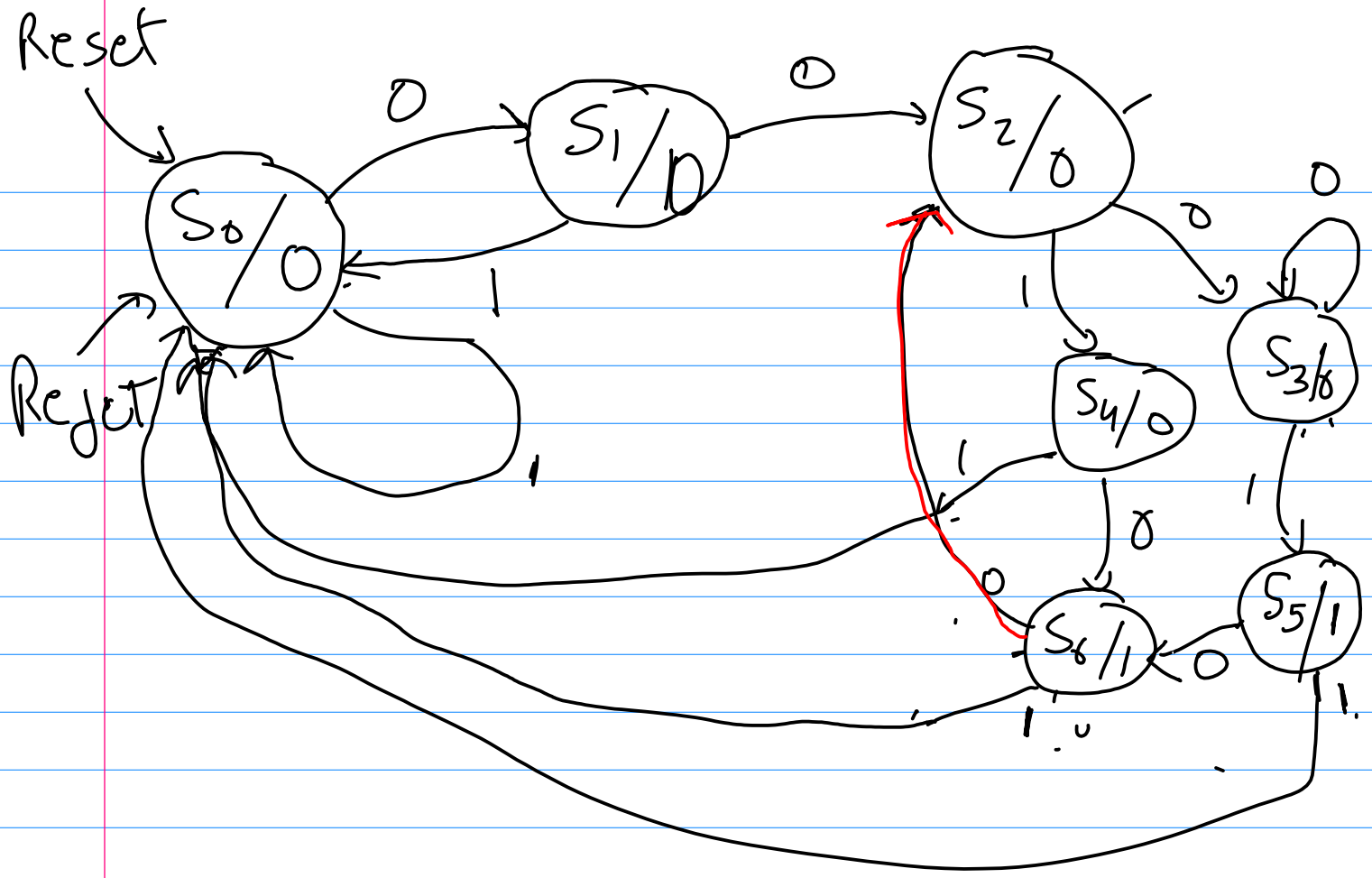


Moore



2-minutes





State representation → Next state assignment →

S_0	
S_1	0
S_2	00
S_3	000
S_4	001
S_5	0001
S_6	0010

S_6 00100

0010

0001

State assignment

state = 7

$2^2 < 7 \leq 2^3$

ff = 3

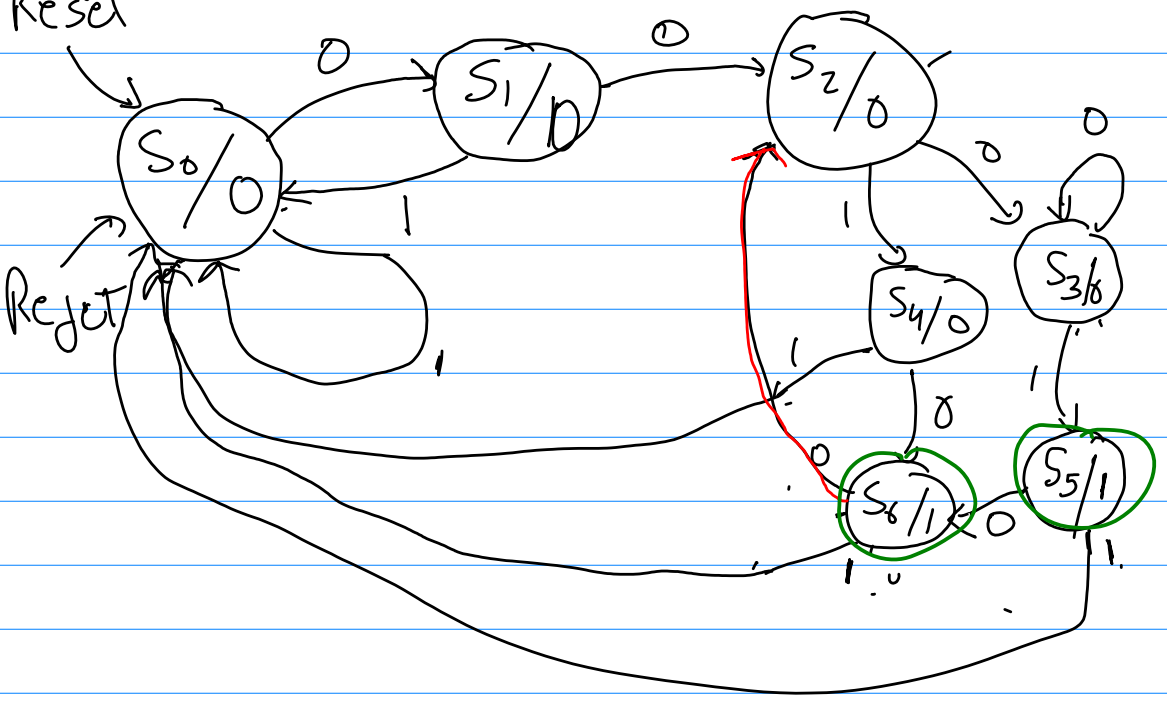
Random assignment

	Q_2	Q_1	Q_0
S_0	0	0	0
S_1	0	0	1
S_2	0	1	0
S_3	0	1	1
S_4	1	0	0
S_5	1	0	1
S_6	1	1	0

$Q_2 = 0$

$Q_1 = 0$

$Q_0 =$



State transition table (with assignments)

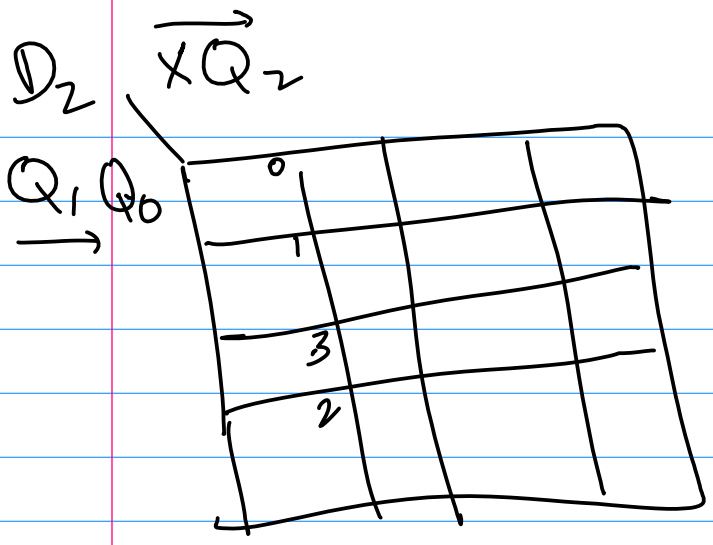
Moore

Input	Present State			Next state			Output
X	Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	Z
0	0	0	0	0	0	1	0
0	0	0	1	0	1	0	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	1	0
0	1	0	0	1	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	1	0	1
0	1	1	1	d	d	d	d
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	1	0	0	0
1	0	1	1	1	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	0	1
1	1	1	0	d	d	d	1
1	1	1	1	d	d	d	d

D-ff

Q	Q^*	D
0	0	0
0	1	1

Input	Present State			D-input			Output
X	Q_2	Q_1	Q_0	D_2	D_1	D_0	Z
0	0	0	0	0	0	1	0
0	0	0	1	0	1	0	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	1	0
0	1	0	0	1	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	1	0	1
0	1	1	1	d	d	d	d
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	1	0	0	0
1	0	1	1	1	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	0	1
1	1	1	0	0	0	0	1
1	1	1	1	d	d	d	d

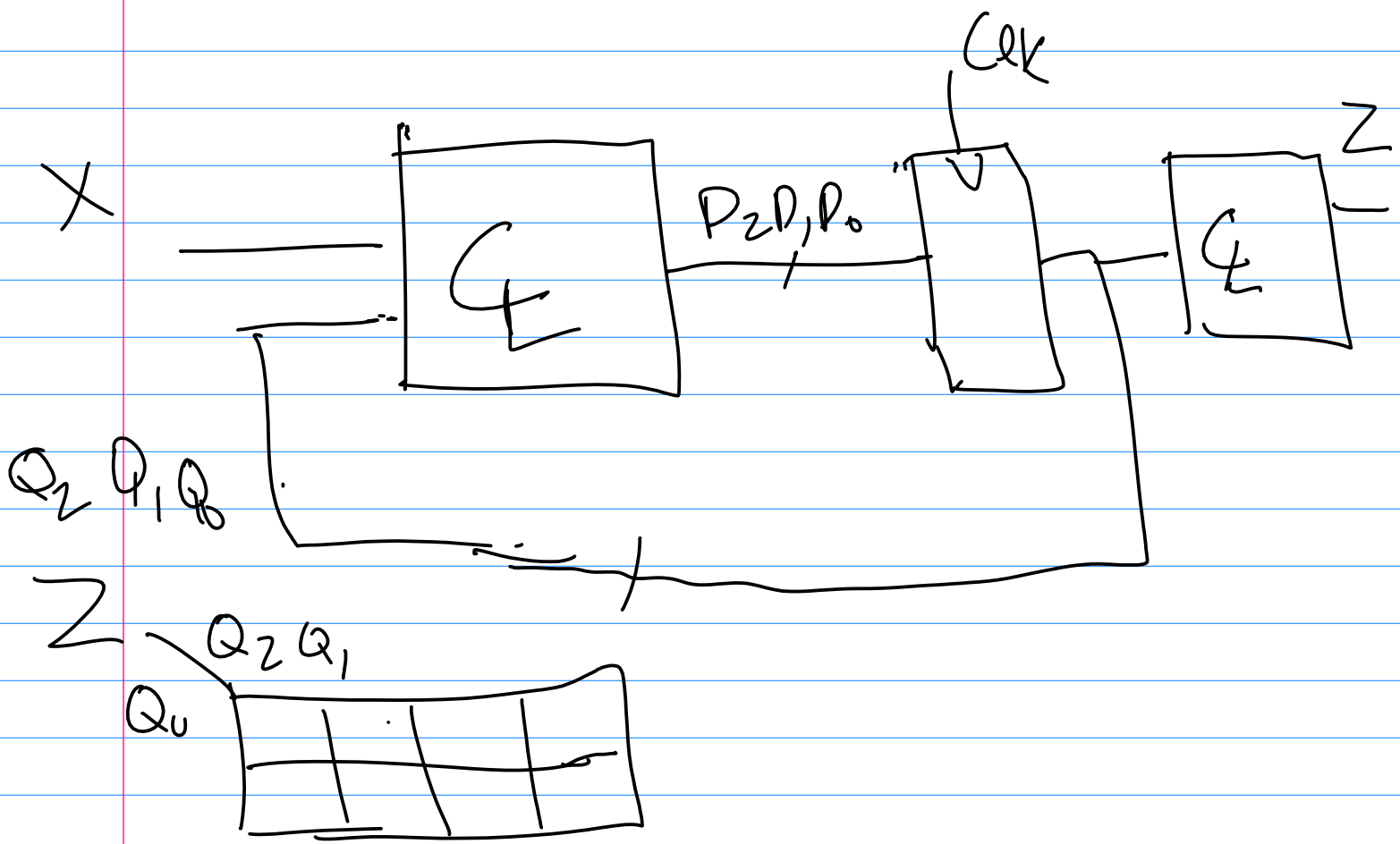

D_2
$\overrightarrow{XQ_2}$
$Q_1 Q_0$
0
1
3
2

$D_2 = ?$

$D_1 = ?$

$D_0 = ?$

$Z = ?$


CLK
X
Z
$P_2 P_1 P_0$
CL
CL
$Q_2 Q_1 Q_0$

Z

$Q_2 Q_1$
Q_0

Design circuit using JK ff