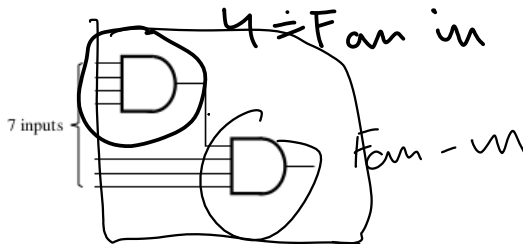# Sequential logic design: More terminology

Vikas Dhiman for ECE275

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Definition 1 (Fan-in). *The fan-in of a logic gate is number of inputs to a logic gate. [2, Section B.8.9]*


Remark 1 (Fan-in). *The fan-in of a gate is limited by the propagation delay t_p. Higher the fan-in, higher the t_p. The output voltage thresholds like V_{OL} and V_{OH} also limit fan-in. Higher the fan-in, higher is V_{OL} (and lower is the V_{OH}).*

Example 1. *Implement an OR gate with fan-in of 7 using OR gates with fan-in of 3.*
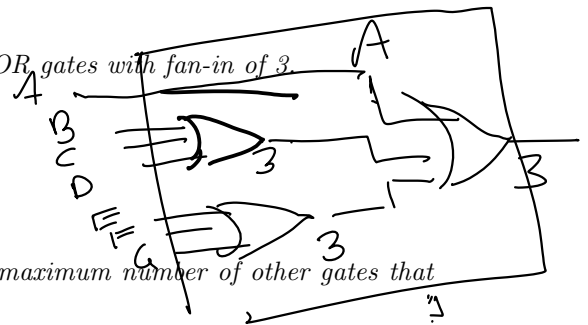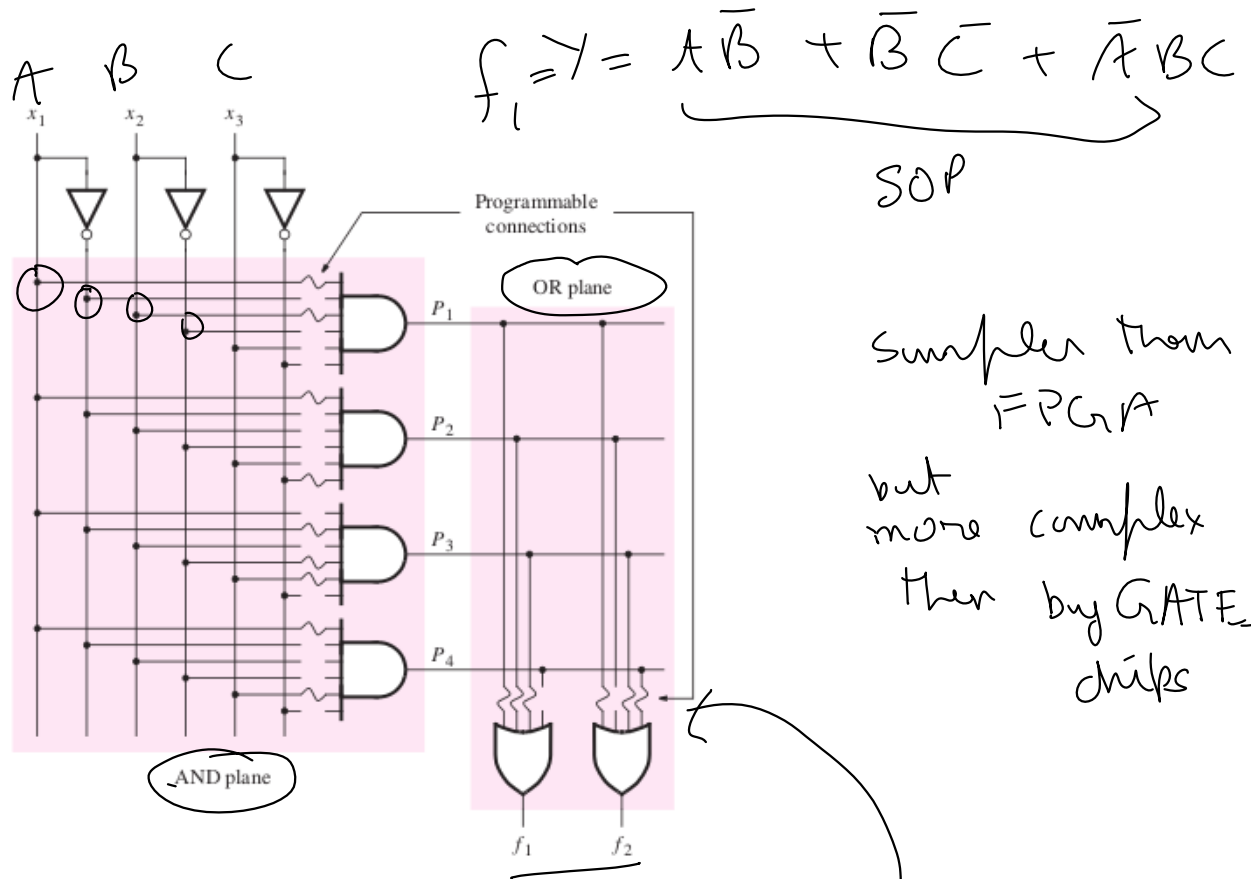

Definition 2 (Fan-out). *The fan-out of a logic gate is the maximum number of other gates that can be connected to output of a gate. [2, Section B.8.9]*
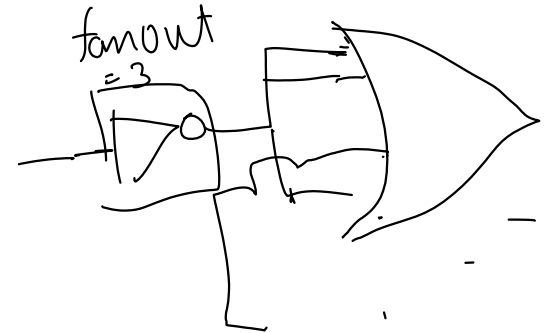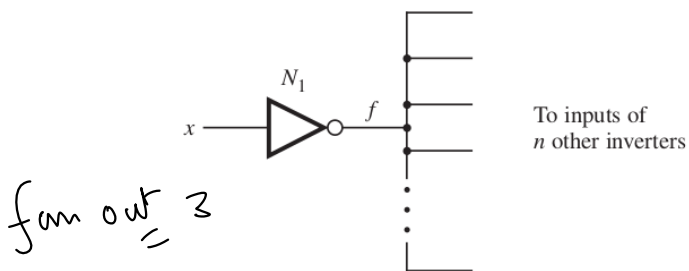
Definition 3 (Programmable Logic Array (PLA)). *Structure of a PLA:*

AND-OR PLA

A   B   C $f_1 = y = A\bar{B} + \bar{B}\bar{C} + \bar{A}BC$

x_1 x_2 x_3 SOP

Programmable
connections

OR plane

P_1

P_2

P_3

P_4

AND plane

f_1 f_2

simpler than
FPGA

but
more complex
then by GATES
chips

Programmable switches

Figure B.26 Gate-level diagram of a PLA.   [2, Section B.6.1]

Definition 4 (Programmable Array Logic (PAL)). *Structure of a PAL:*

x_1 x_2 x_3

P_1

P_2 f_1

P_3

P_4 f_2
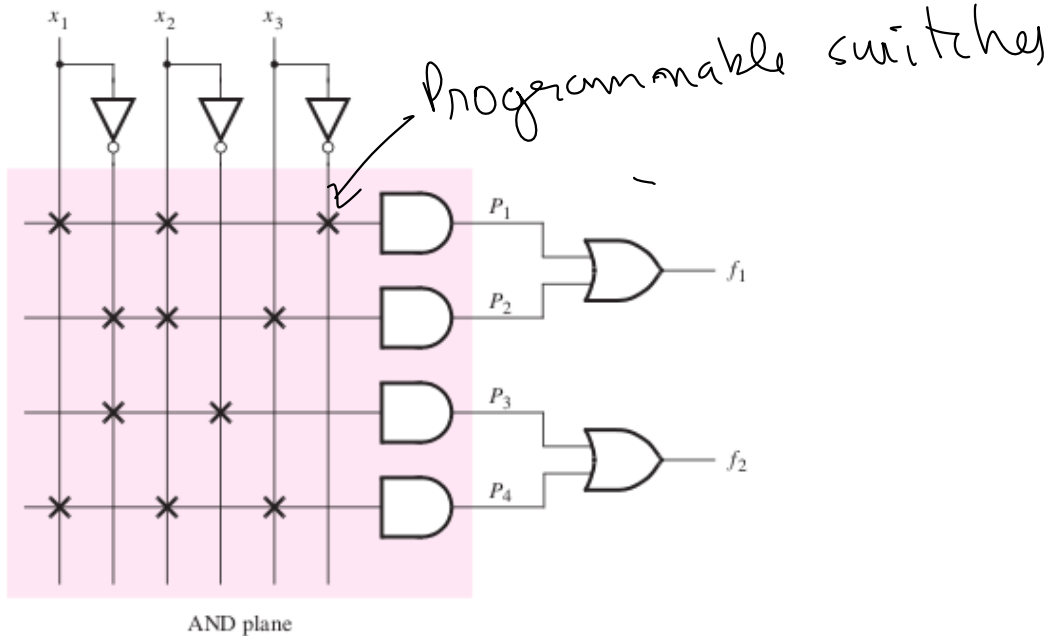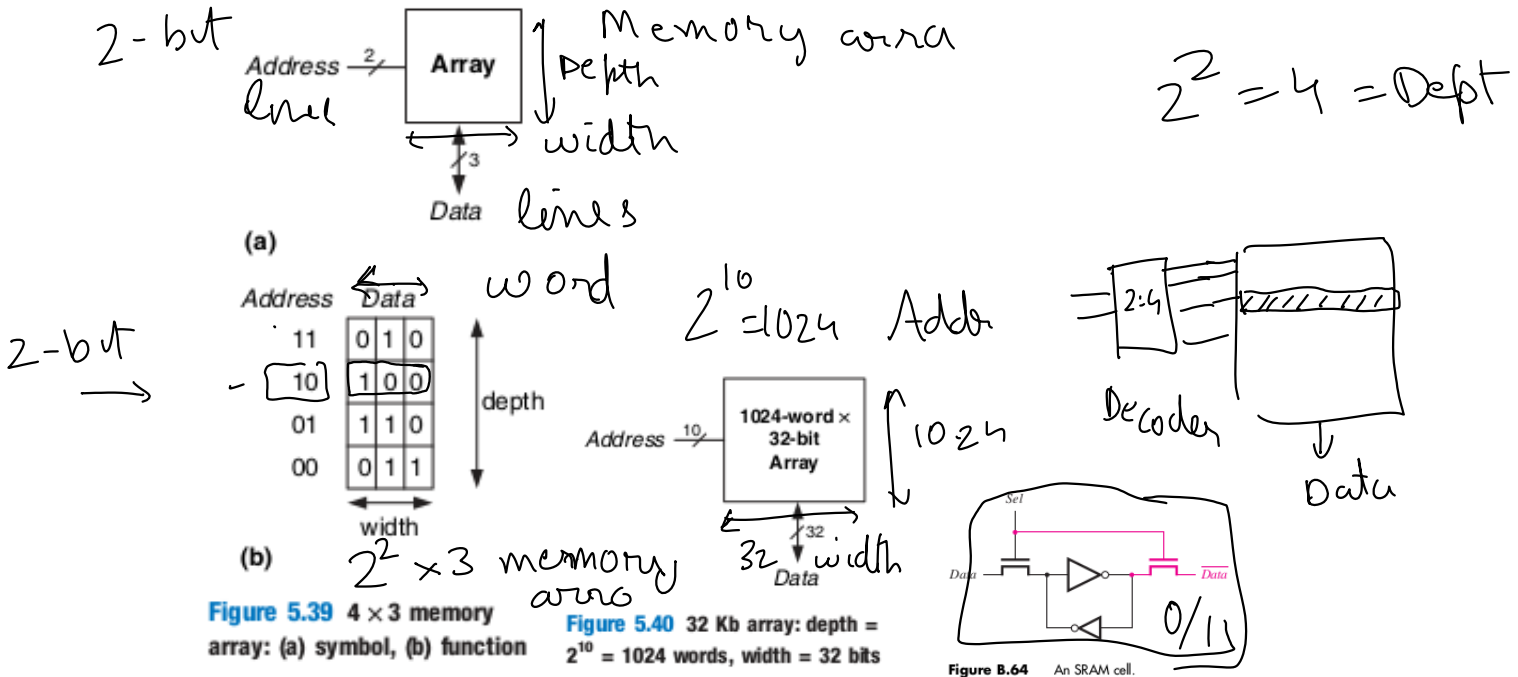
AND plane

Figure B.28 An example of a PAL.

[2, Section B.6.2]

Example 2. *What is the difference between PLA and PAL?*

2

Definition 5 (Random Access Memory (RAM)). *Structure of a RAM is as follows:*

2-bt lines

2² = 4 = Dept

Memory area
Depth
width
lines

Address —2/→ **Array**
/3
Data

(a)

2-bt →

2² × 3 memory area

$2^{10} = 1024$ Addr

Address	Data		
11	0	1	0
10	1	0	0
01	1	1	0
00	0	1	1

depth
width
(b)

Figure 5.39 4 × 3 memory array: (a) symbol, (b) function

Address —10/→ **1024-word × 32-bit Array**
1024
32 width
/32
Data

32 width

Figure 5.40 32 Kb array: depth = 2^{10} = 1024 words, width = 32 bits

2:4 Decoder
Data

Sel
Data — Data
0/1

Figure B.64 An SRAM cell.

RAM

Random as opposed Sequential

Data inputs { d_{n-1} d_{n-2} ⋯ d_0

Write

m-bt 0
Address { a_0, a_1, ⋯ a_{m-1} }
0

Sel₀
Sel₁ 0/1 0/1 ⋯ 0/0
Sel₂
⋯
Sel_{2^m-1}

m-to-2^m decoder

=1 Read

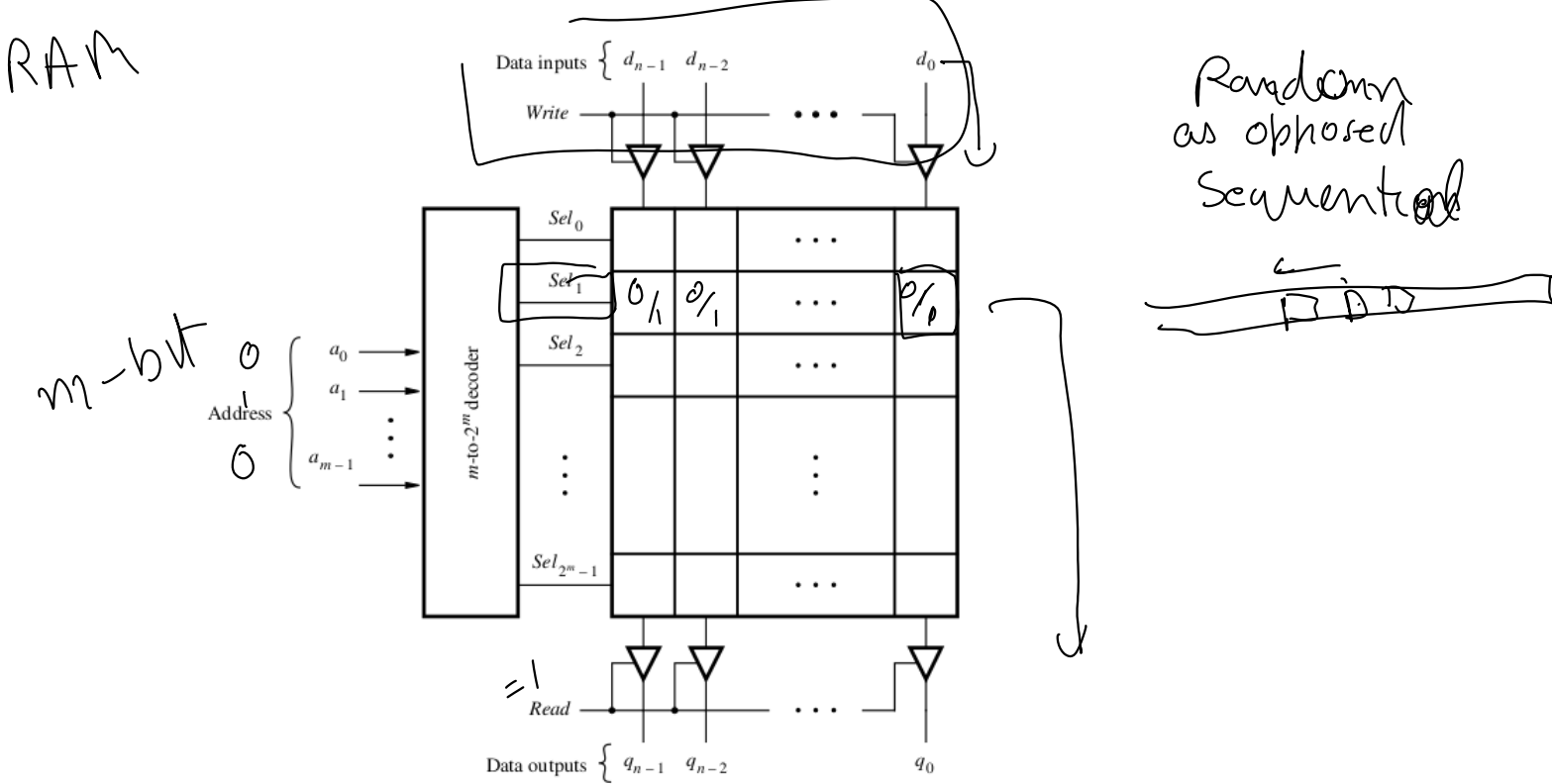Data outputs { q_{n-1} q_{n-2} ⋯ q_0

Figure B.66 A $2^m \times n$ SRAM block.

Definition 6 (Read Only Memory (ROM)). *Structure of a ROM is as follows:*
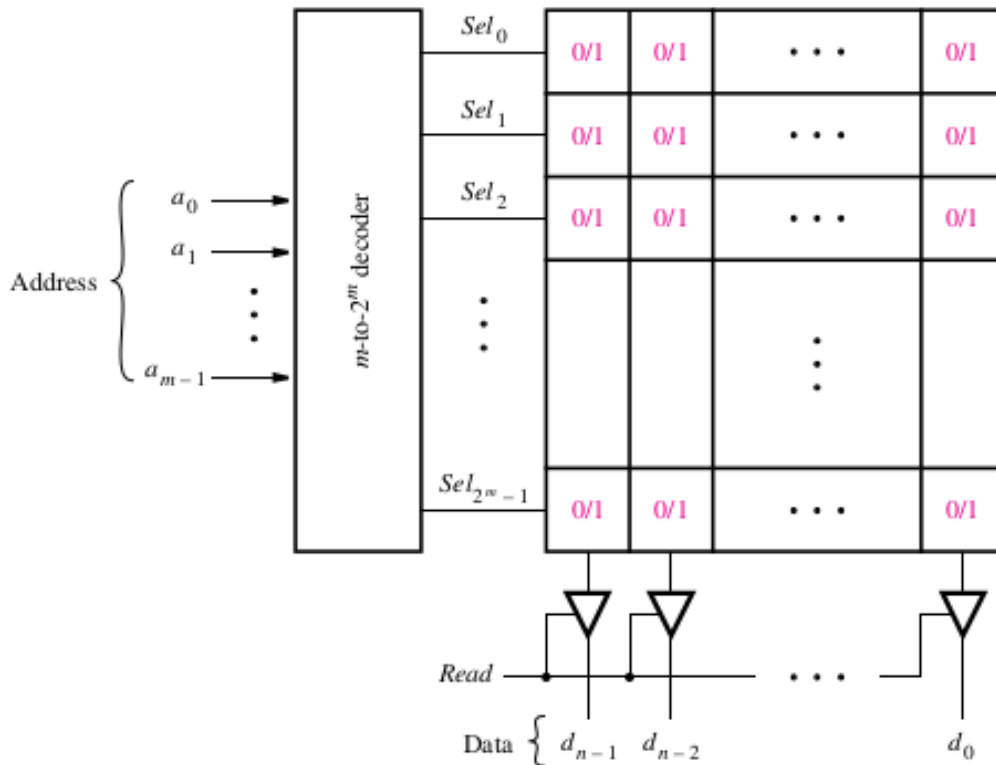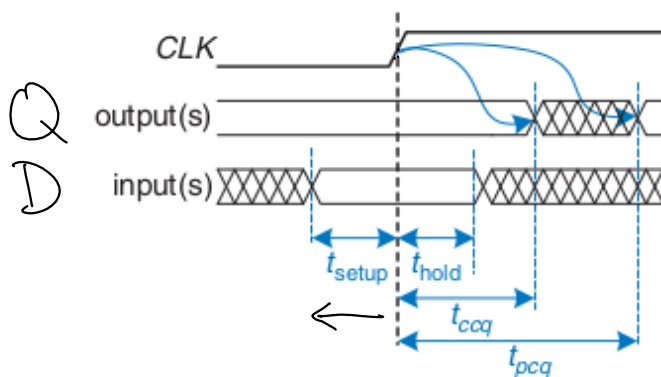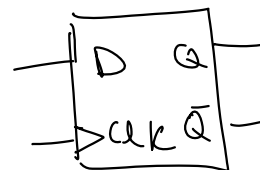
3

Figure B.72   A $2^m \times n$ read-only memory (ROM) block.

e.g. a ff

1   Timing parameters for sequential circuit [1, Section 3.5]

t_p = prop delay

t_c = contamination delay

t_{ccq} = clock to Q contamination delay

t_{pcq} = clock to Q propagation delay

Definition 7 (Setup time t_{su} of a latch/flip-flop). *Time for which input must be stable before the clock edge.*

Definition 8 (Hold time t_h of a latch/flip-flop). *Time for which input must be stable after the clock edge.*

4

Definition 9 (Clock-to-Q contamination delay t_{ccq} of a latch/flip-flop). *Time taken to influence (contaminate) the Q output after the clock edge.*

Definition 10 (Clock-to-Q propagation delay t_{ccq} of a latch/flip-flop). *Time taken for Q output to stabalize after the clock edge.*

2 FPGA [2, Section B.6.5]
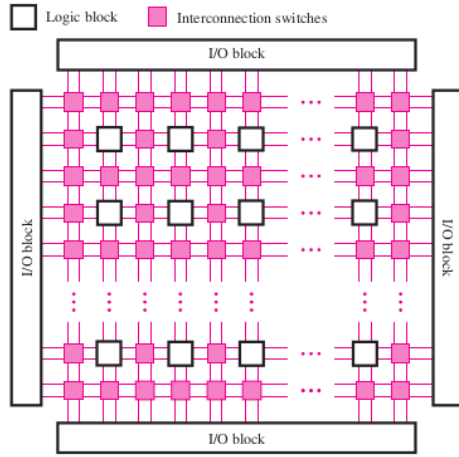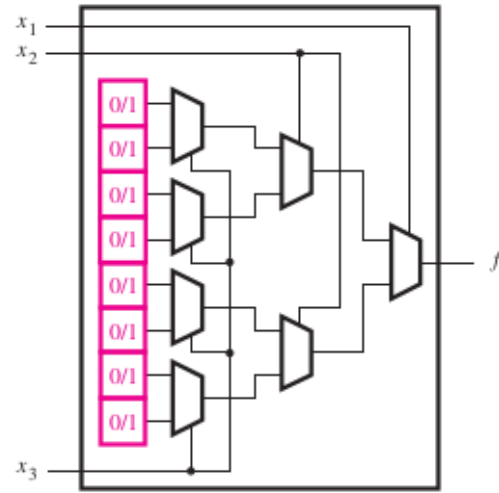

(a) General structure of an FPGA

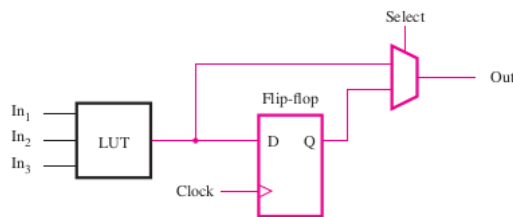**Figure B.37**   A three-input LUT.

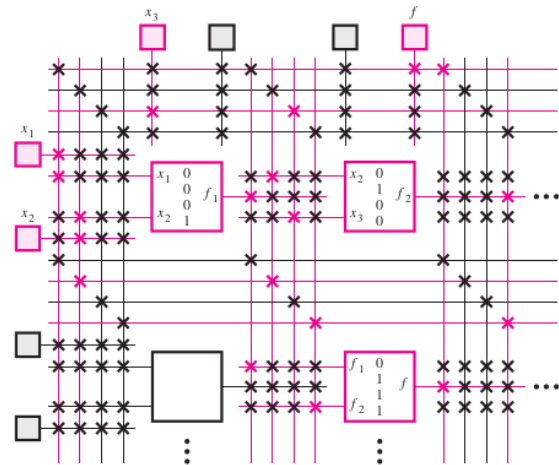**Figure B.38**   Inclusion of a flip-flop in an FPGA logic element.

Figure B.39   A section of a programmed FPGA.

References

[1] Sarah L Harris and David Harris. *Digital design and computer architecture*. Morgan Kaufmann, 2022.

[2] Brown Stephen and Vranesic Zvonko. *Fundamentals of digital Logic with Verilog design*. McGraw Hill, 2022.