

1 Study guide

1.1 Midterm 1

- ✓ Binary numbers, Hexadecimal, Sign-magnitude, One's-complement and Two's complement. Conversions between them.

1. Homework 1 and Lectures 08/31 and 09/02.

- ✓ Generate minterms, maxterms, SOP canonical form and POS canonical forms and convert between them

1. Lecture 09/09

- ✓ Understand and use the laws and theorems of Boolean Algebra

1. Homework 2 and Lectures 09/16-09/19

- ✓ Perform algebraic simplification using Boolean algebra

1. Homework 2 and Lectures 09/16-09/19

- ✓ Simplification using K-maps (upto 5-input variables)

1. Homework 2 and 3 and Lectures 09/12-09/14

- ✓ Derive sum of product and product of sums expressions for a combinational circuit

1. Homework 2 and 3 and Lectures 09/12-09/23

- ✓ Convert combinational logic to NAND-NAND and NOR-NOR forms

1. Homework 3 and Lecture 09/28

1.2 Midterm 2

- ✓ Simplification using Quine-McCluskey method

1. Lecture 09/28

- ✓ Design combinational circuits for positive and negative logic

1. For Negative logic is $H = 0$, $L = 1$. See Example 6, on lecture 10/19

- ✓ Design Hazard-free two level circuits.

1. See Example 14, on lecture 10/24

- ✓ Design a CMOS complex gate

- 1. Lecture 10/24
- Compute noise margin of one device
 - 1. See Section 2 of lecture 10/17
- Describe how tri-state and open-collector outputs are different from totem-pole outputs.
 - 1. See Definitions 11-13 covered in lecture 10/21
- Different between and limitations of level-triggered latches and edge-triggered flip-flops.
 - 1. See lecture 10/26-10/28
- Understand the difference between synchronous and asynchronous inputs
 - 1. See lecture 10/26-10/28
- Derive a state graph or state table from a word description of the problem
 - 1. Lecture 11/02
- Implement a design using JK, SR, D or T flip-flops
 - 1. Lecture 10/02
- Analyze a sequential circuit and derive a state-table and a state-graph

1.3 Final (includes previous topics)

- Reduce the number of states in a state table using row reduction and implication tables
 - 1. Lecture 11/30
- Perform a state assignment using the guideline method
 - 1. Lecture 12/02
- Analyse and design both Mealy and Moore sequential circuits with multiple inputs and multiple outputs
 - 1. Lecture 11/28
- Design combinational circuits using multiplexers and decoders
 - 1. Lecture 12/05 and 12/07
- Know fan-out and noise margin

1. Lecture 12/07

- Know the differences and similarities between PAL, PLA, and ROMs (

1. Lecture 12/07

- Convert between Mealy and Moore designs
- Partition a system into multiple state machines